


LCFC Confidential

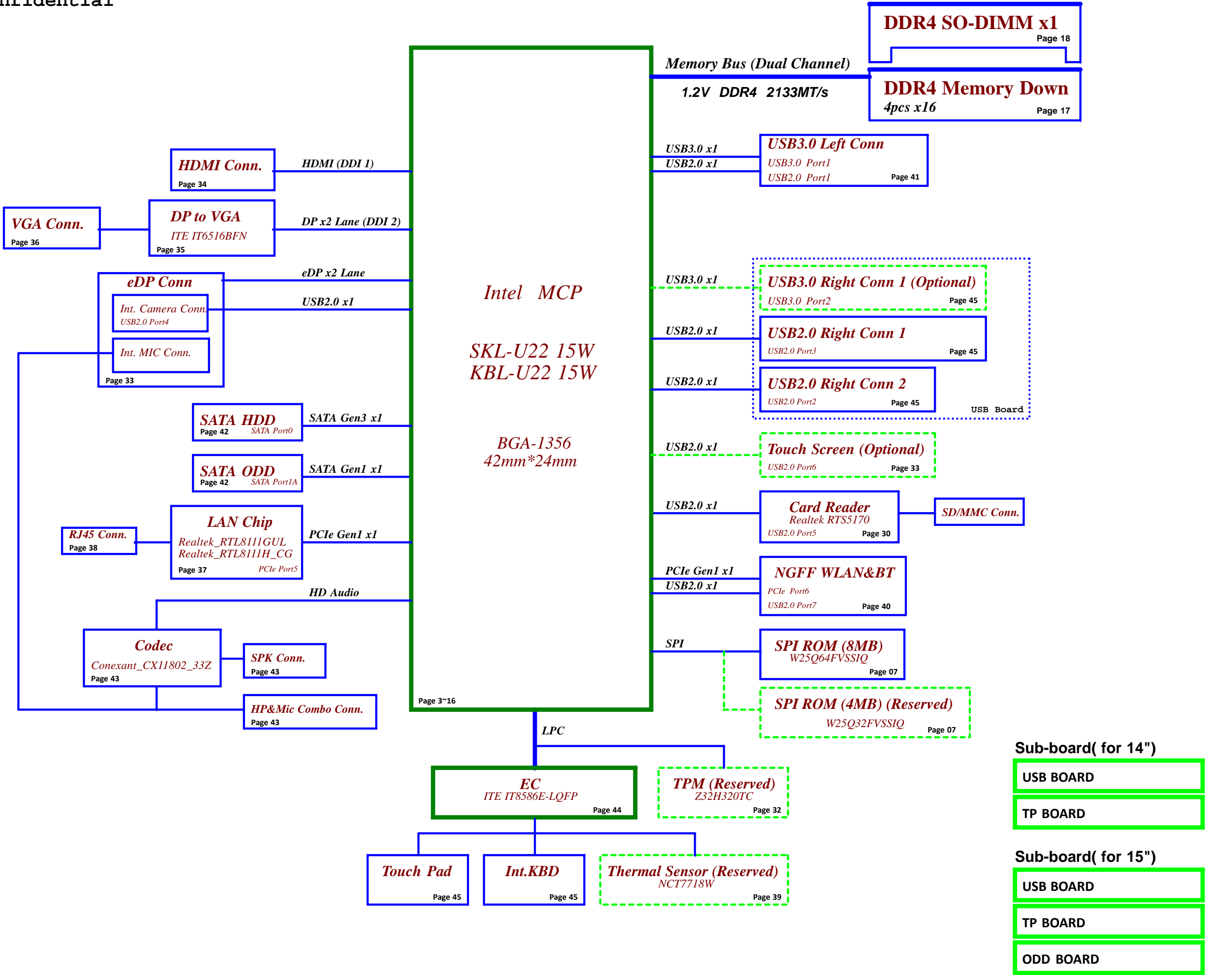
CG411/CG511 MB Schematics Document

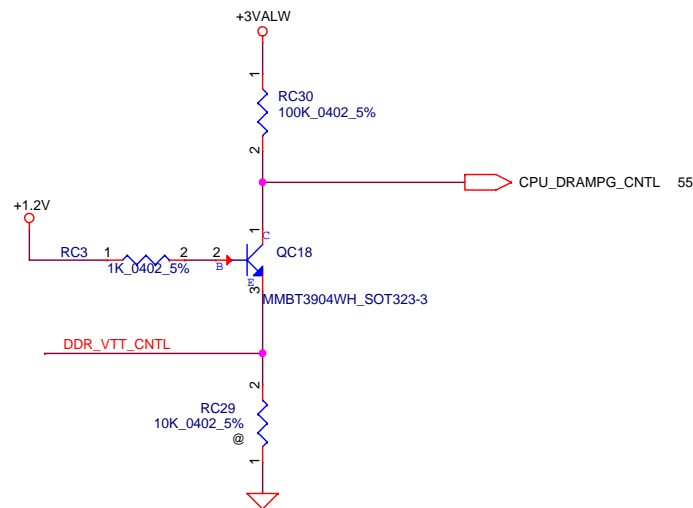
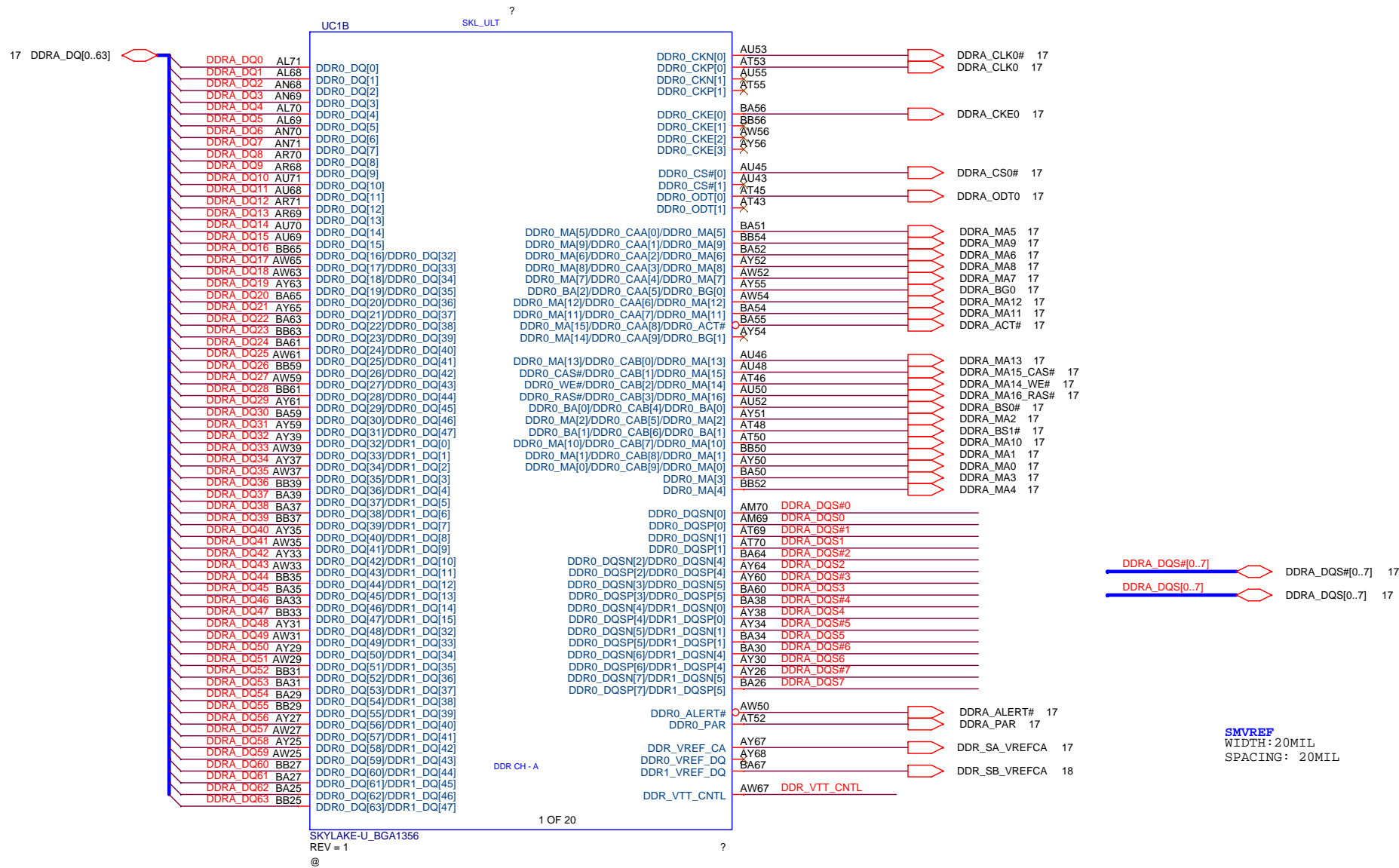
Intel Skylake-U22&U23/Kabylake-U22&U23 with DDR4

2016-01-11

REV:1.0

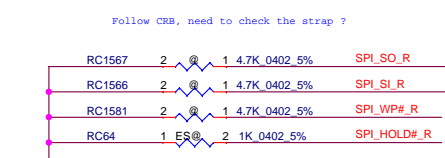
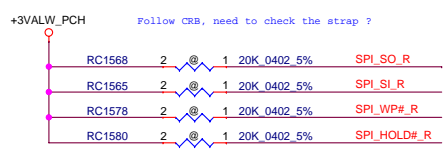
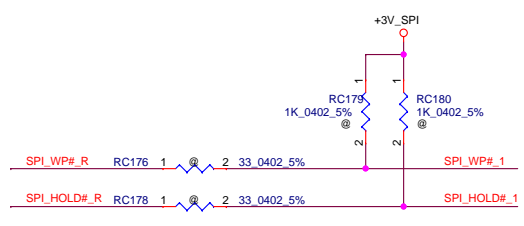
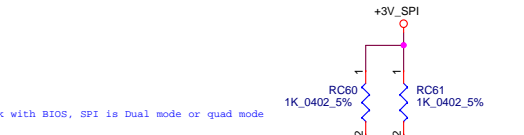
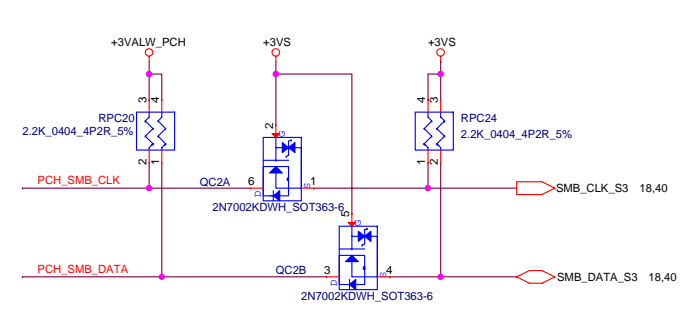
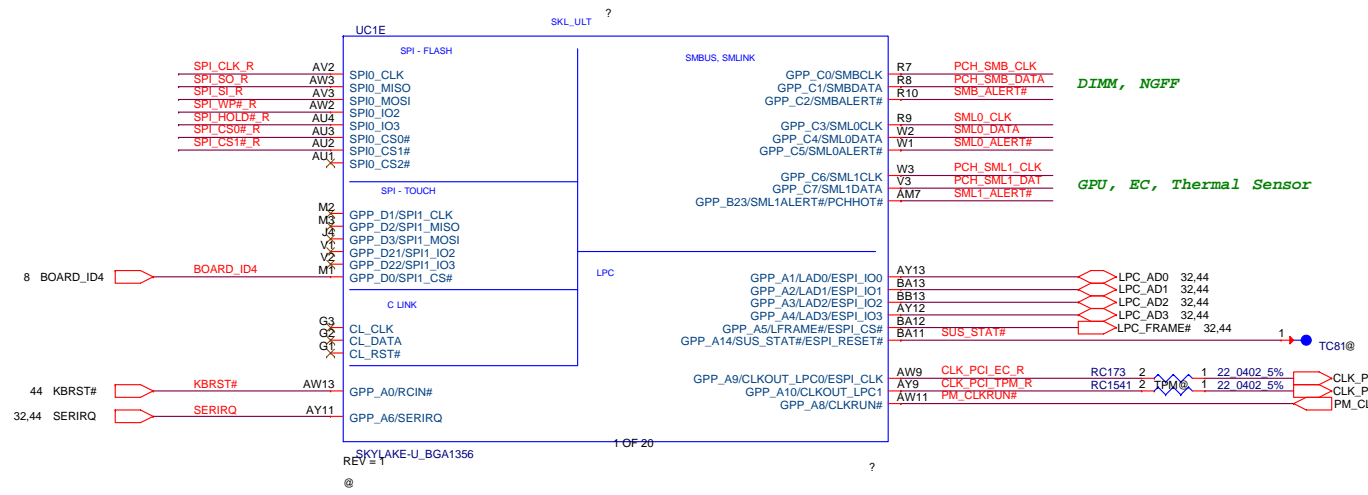
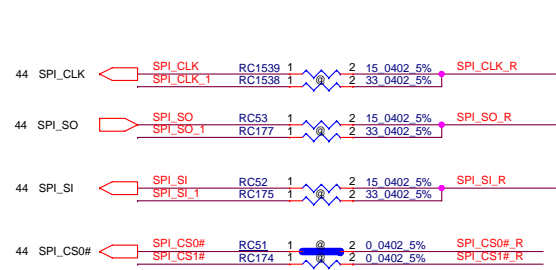
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				Date: Thursday, January 14, 2016	Rev 1.0

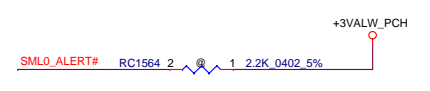
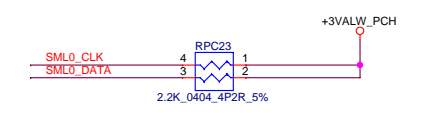
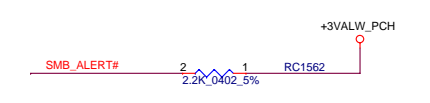
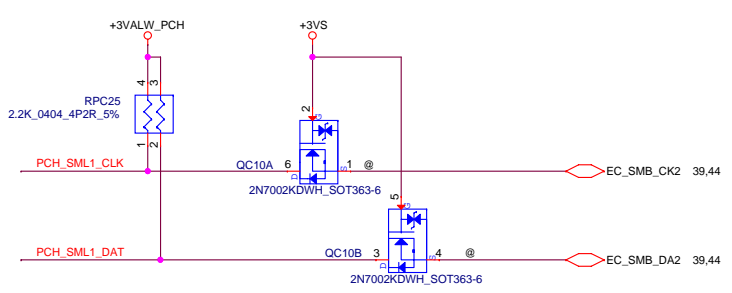
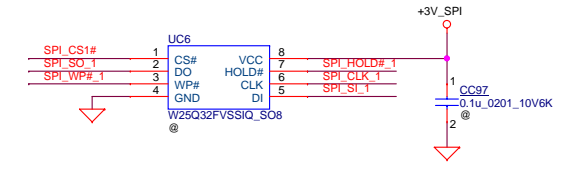
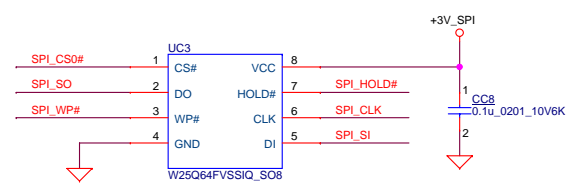
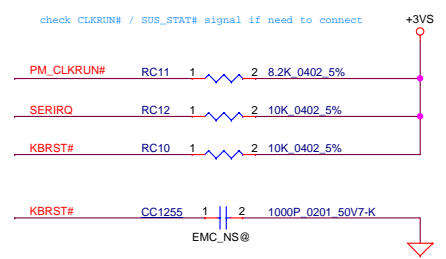




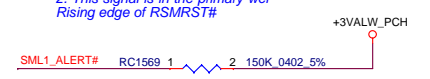
Based on WW36 SKL U&Y WOM, RC64 populated, and RC61 de-populated for SKL U ES sample. In this case, customers must ensure that the SPI flash device on the platform has HOLD functionality disabled by default.

+3V_SPI

1. If support DS3, connect to +3VS and don't support EC mirror code;
2. If don't support DS3, connect to +3VALW_PCH and support EC mirror code.

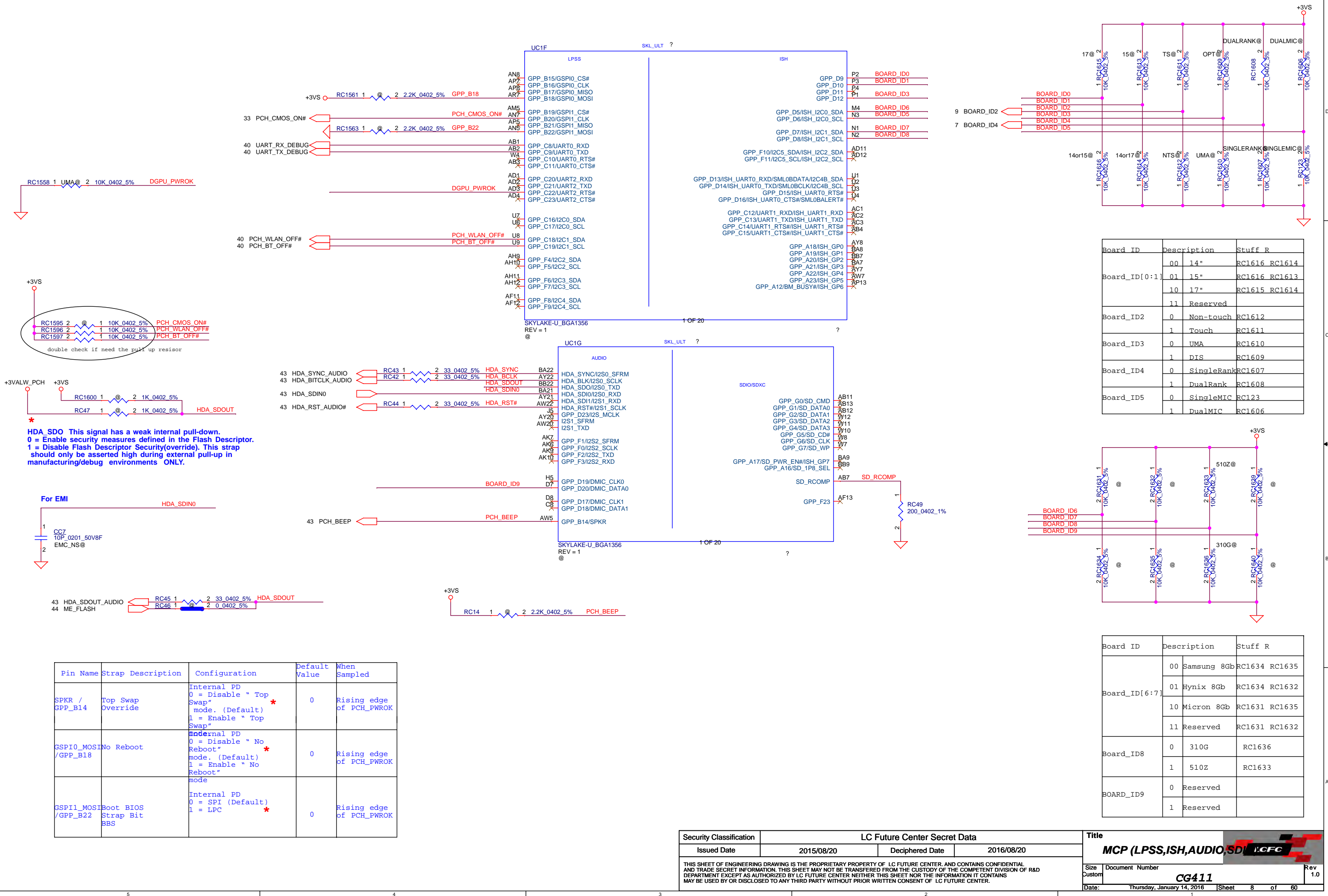


This signal has a weak internal pull-down.
0 = LPC is selected for EC. (Default)
1 = eSPI is selected for EC.
Notes:
1. The internal pull-down is disabled after RSMRST# de-asserts.
2. This signal is in the primary wel
Rising edge of RSMRST#



To enable Direct Connect Interface (DCI), a 150K pull up resistor will need to be added to PCHHOT# pin. This pin must be low during the rising edge of RSMRST# (Refer to WWS2_MOW)

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Board ID	Description	Stuff R
Board_ID[0:1]	00 14"	RC1616 RC1614
	01 15"	RC1616 RC1613
	10 17"	RC1615 RC1614
	11 Reserved	
Board_ID2	0 Non-touch	RC1612
	1 Touch	RC1611
Board_ID3	0 UMA	RC1610
	1 DIS	RC1609
Board_ID4	0 SingleRank	RC1607
	1 DualRank	RC1608
Board_ID5	0 SingleMIC	RC123
	1 DualMIC	RC1606

Board ID	Description	Stuff R
Board_ID[6:7]	00 Samsung 8Gb	RC1634 RC1635
	01 Hynix 8Gb	RC1634 RC1632
	10 Micron 8Gb	RC1631 RC1635
	11 Reserved	RC1631 RC1632
Board_ID8	0 310G	RC1636
	1 510Z	RC1633
BOARD_ID9	0 Reserved	
	1 Reserved	

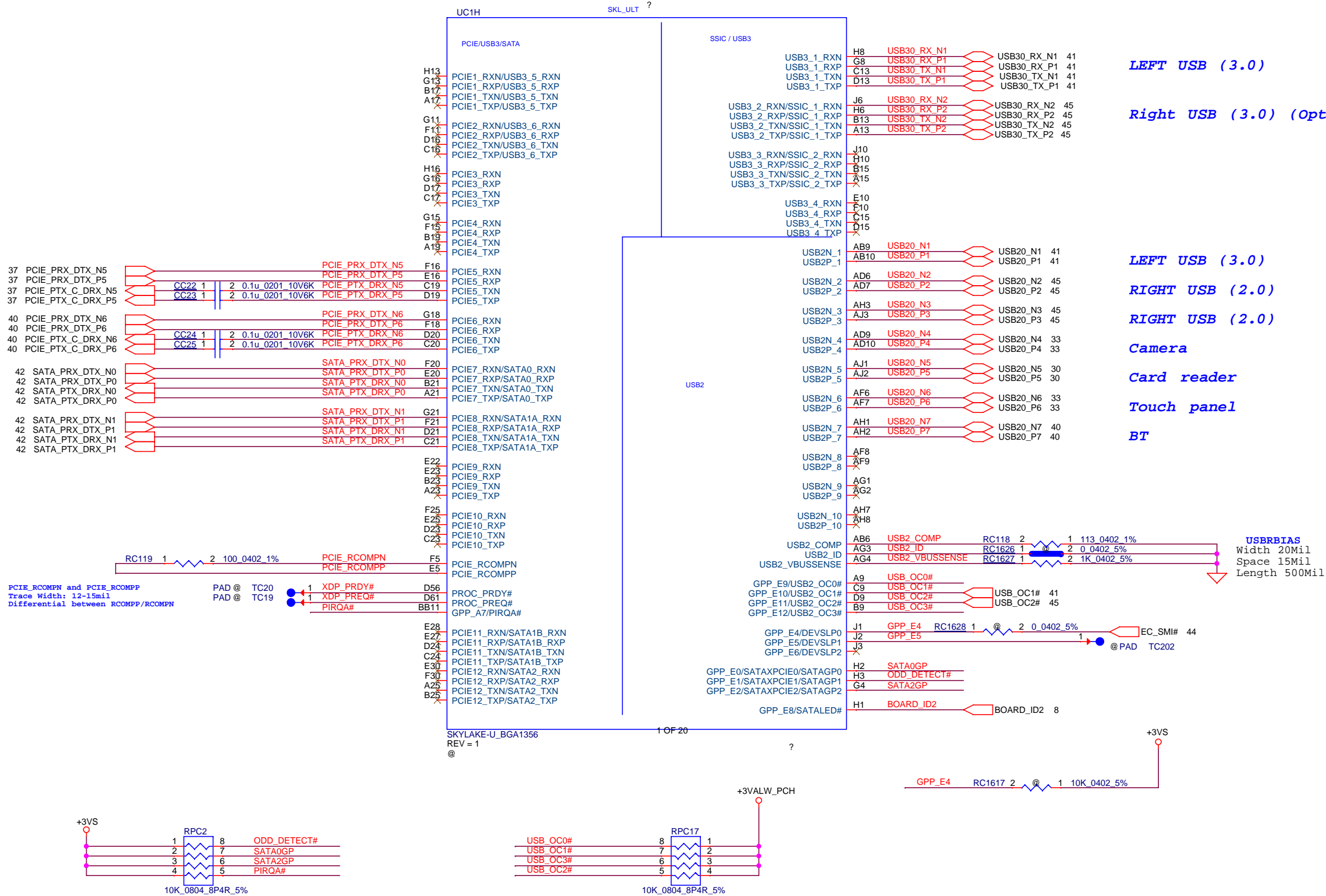
LAN

WLAN

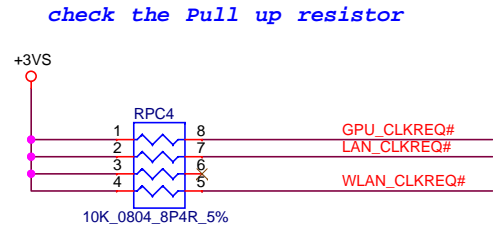
SATA HDD

SATA ODD

DGPU



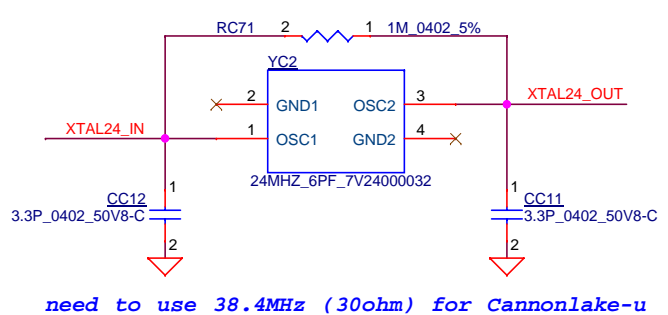
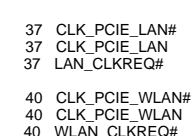
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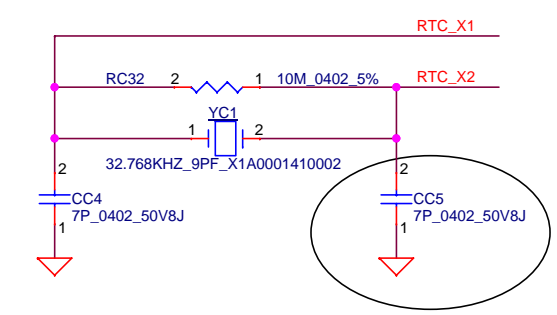
PCIE CLK0 DGPU

PCIE CLK4 LAN

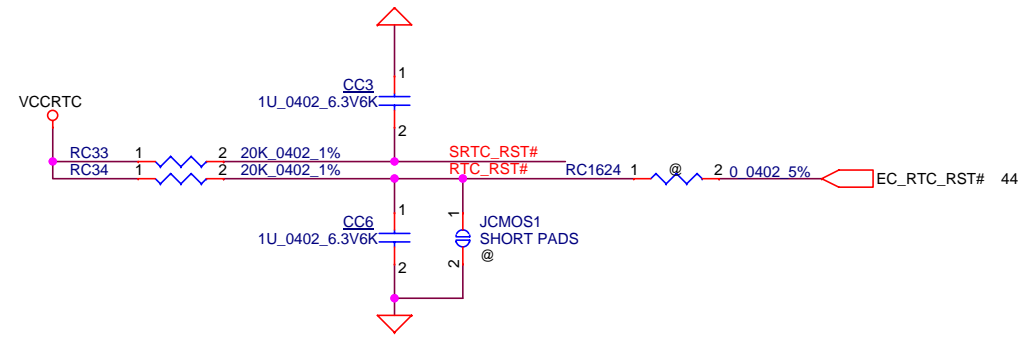
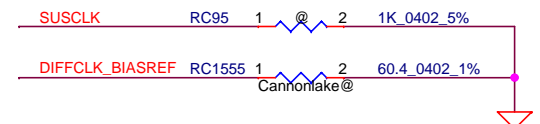
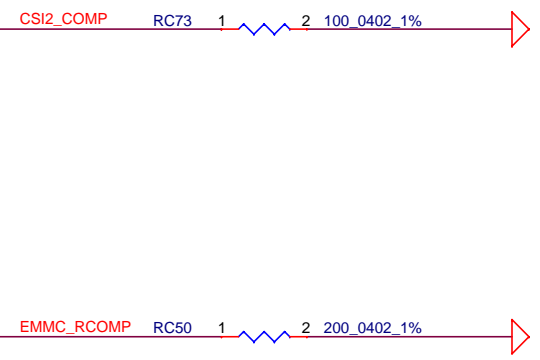
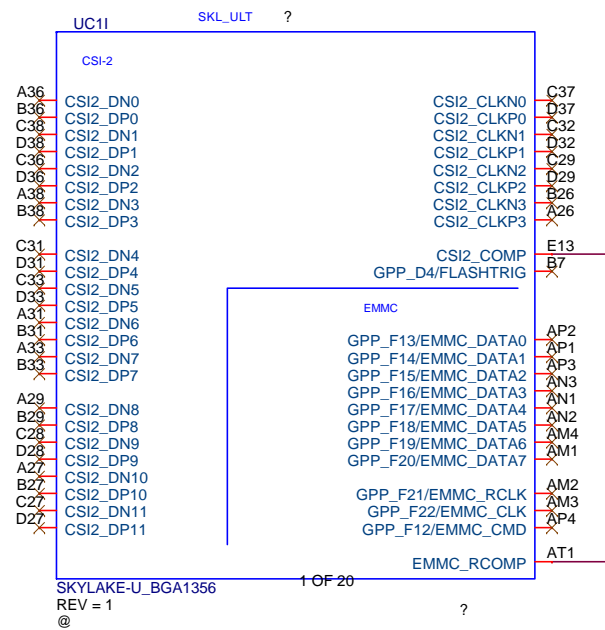
PCIE CLK5 WLAN



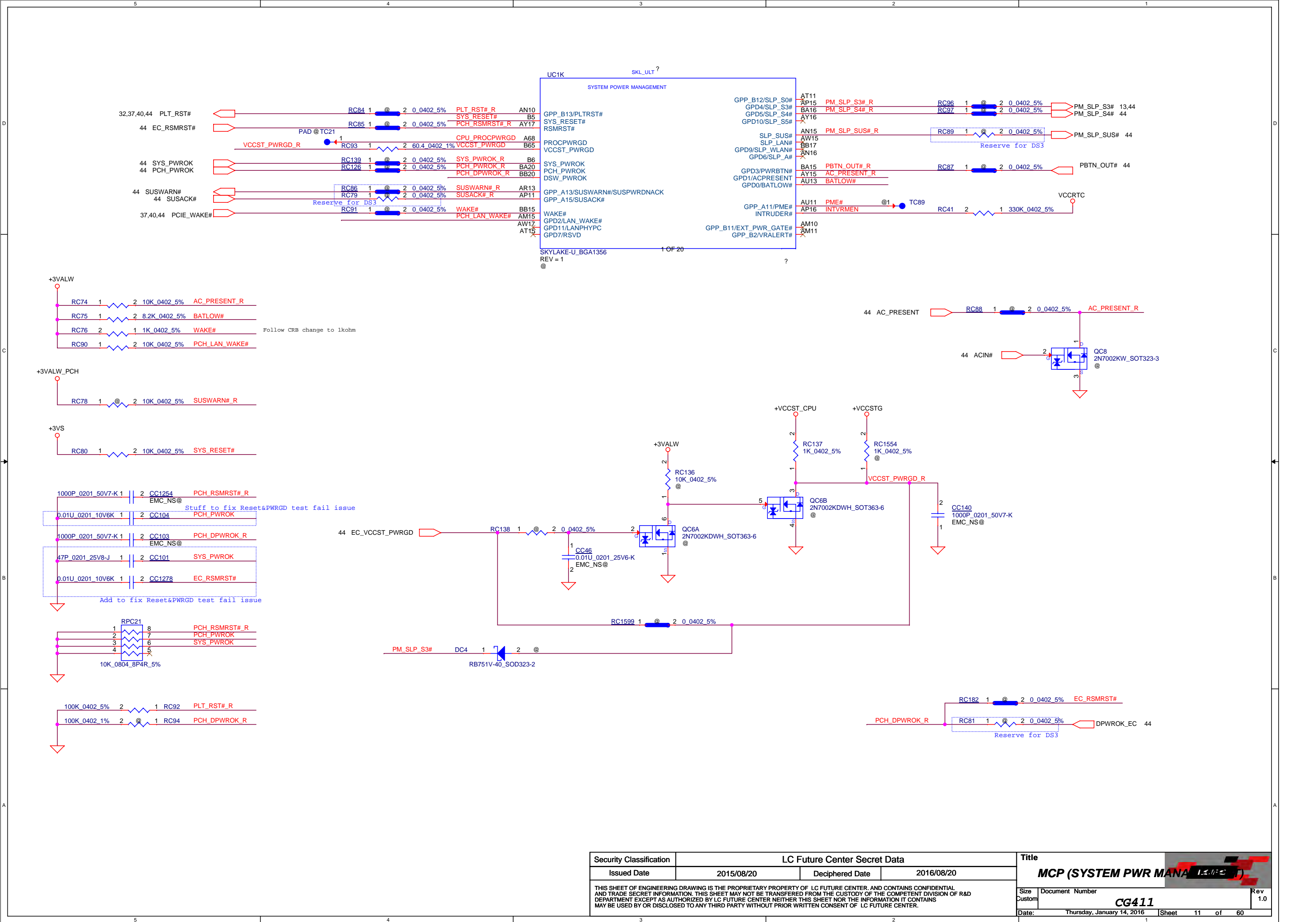
need to use 38.4MHz (30ohm) for Cannonlake-u

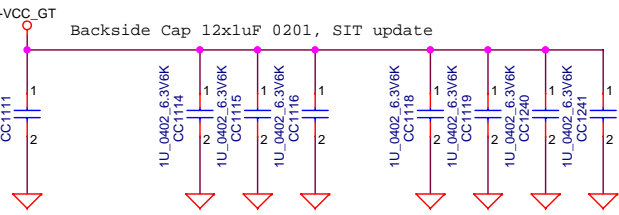
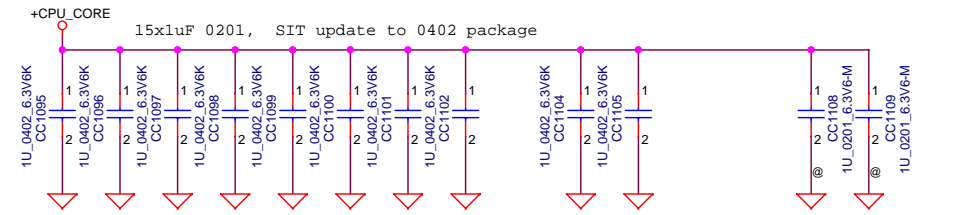
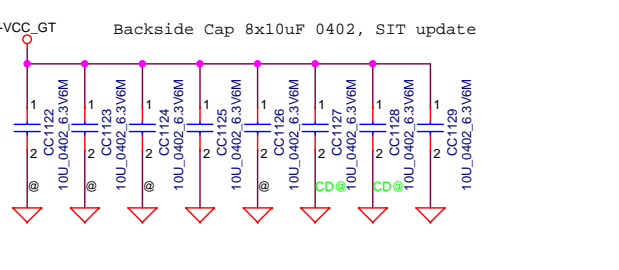
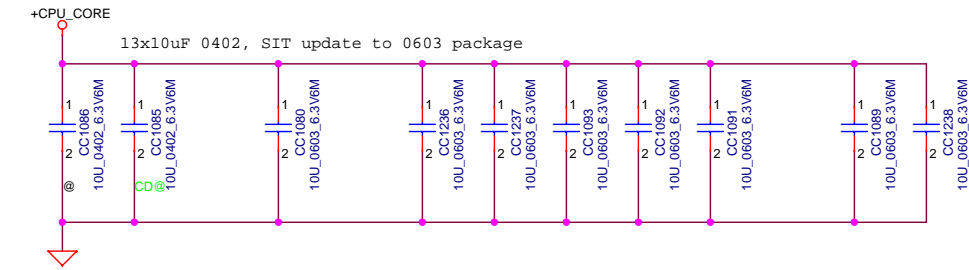
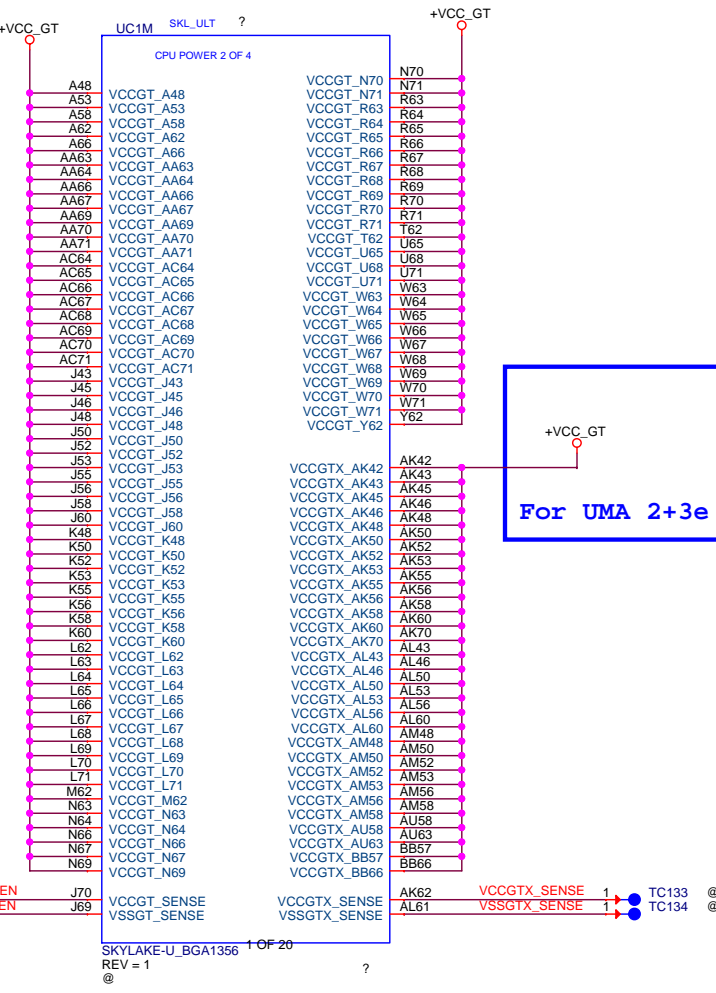
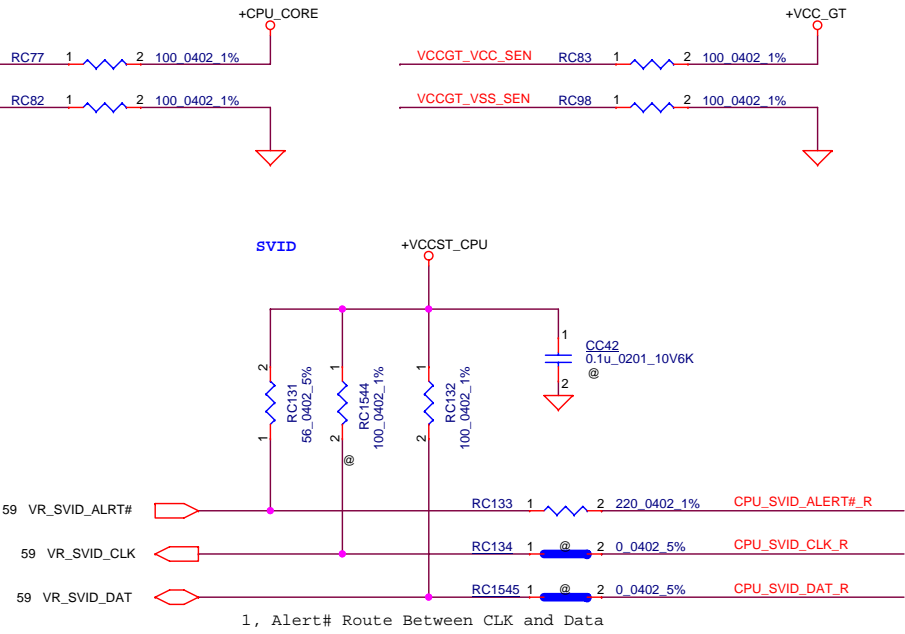
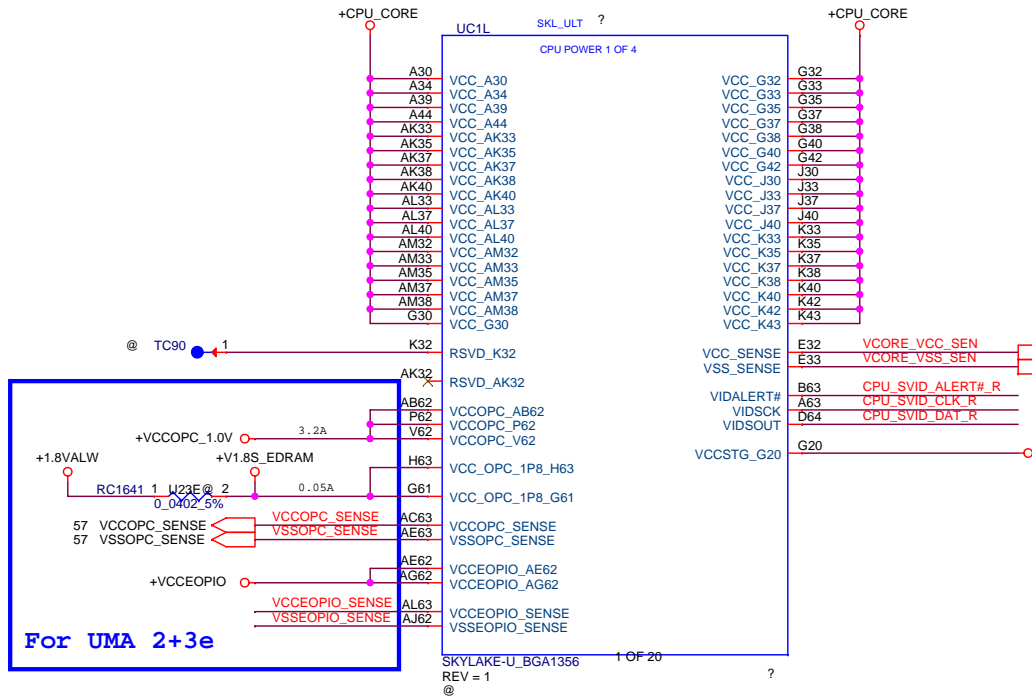


when single end external clock generator used, this pin should be grounded

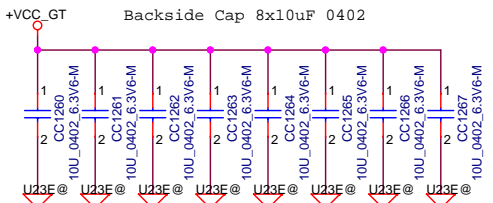
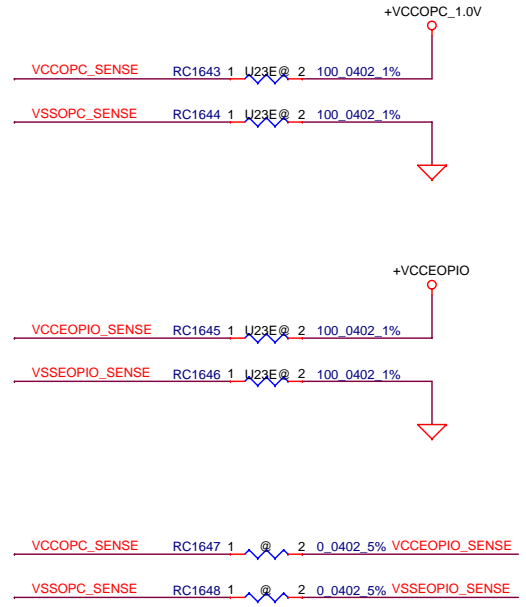
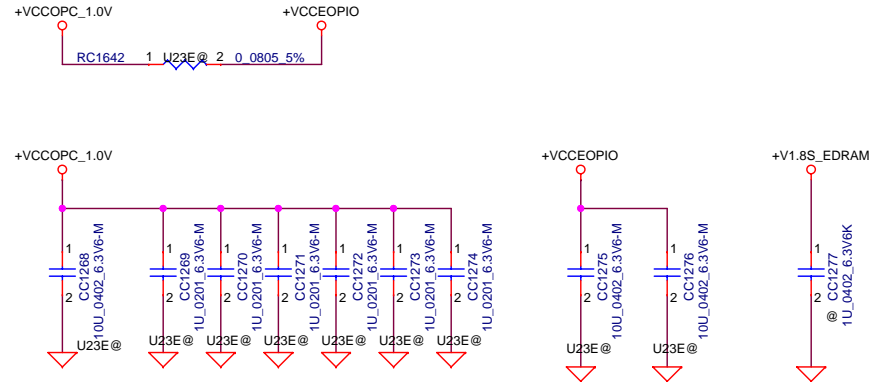



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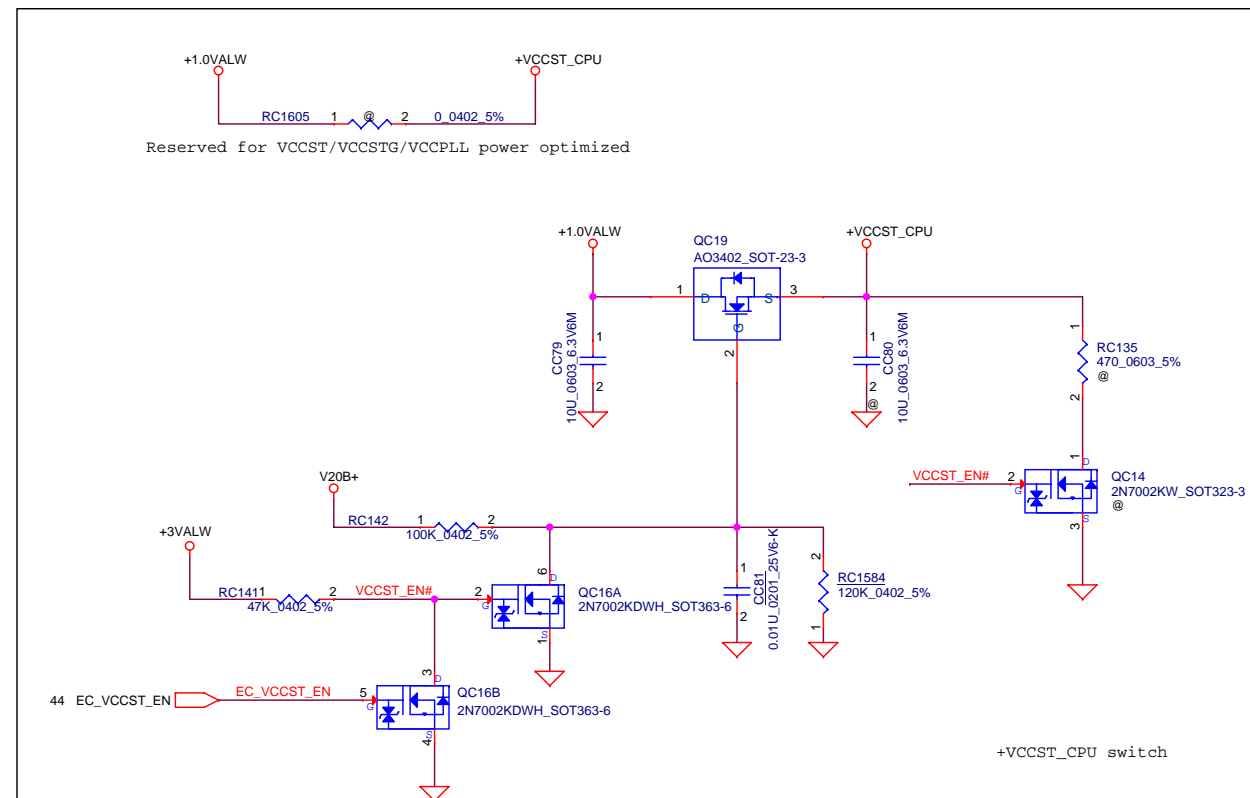
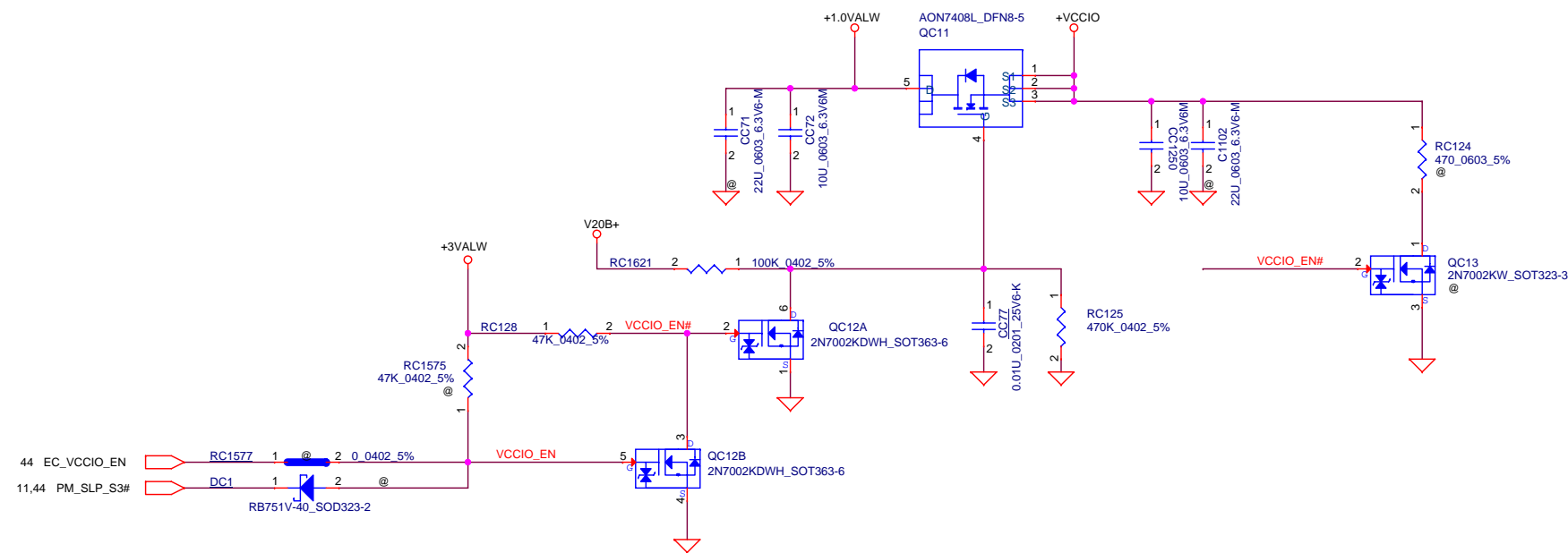
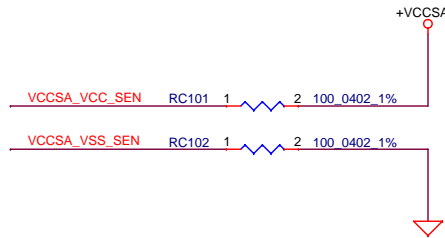
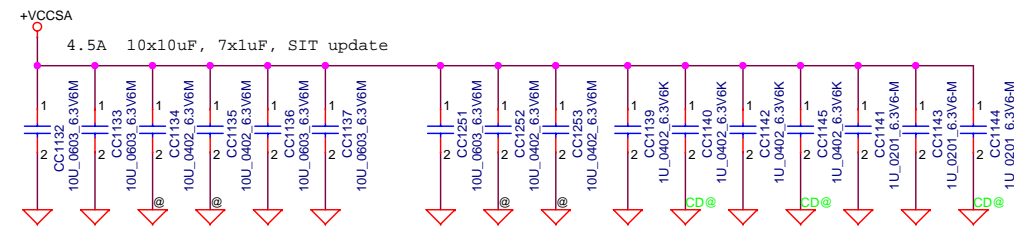
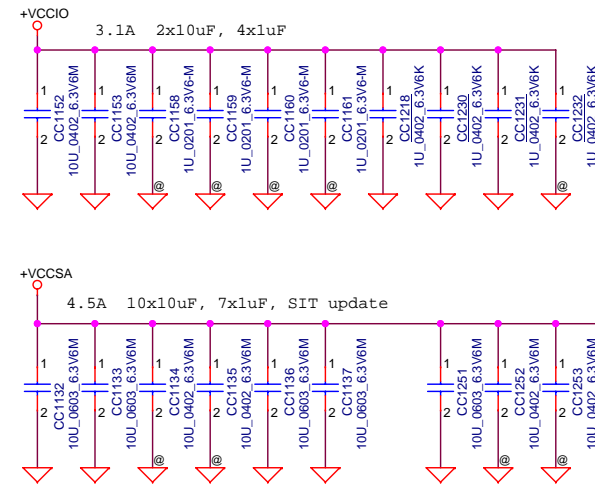
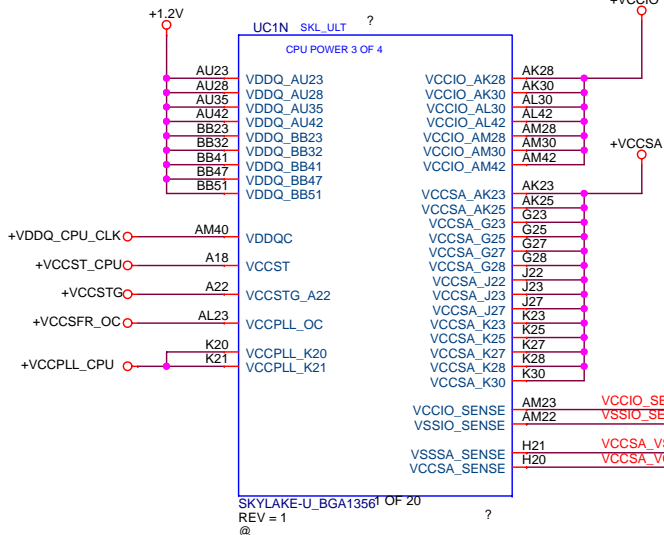
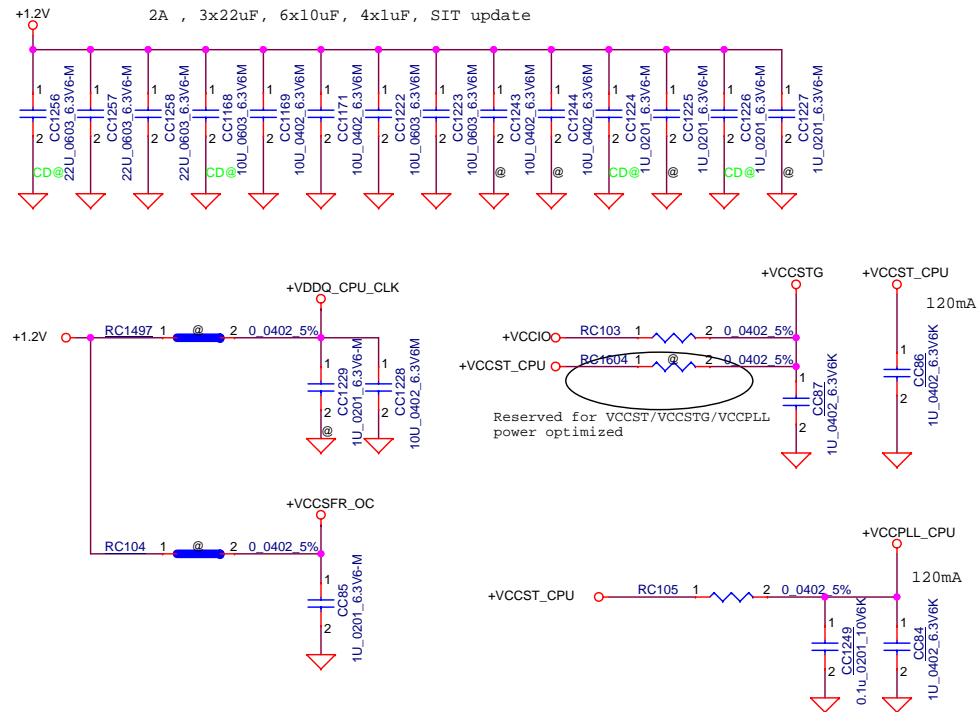





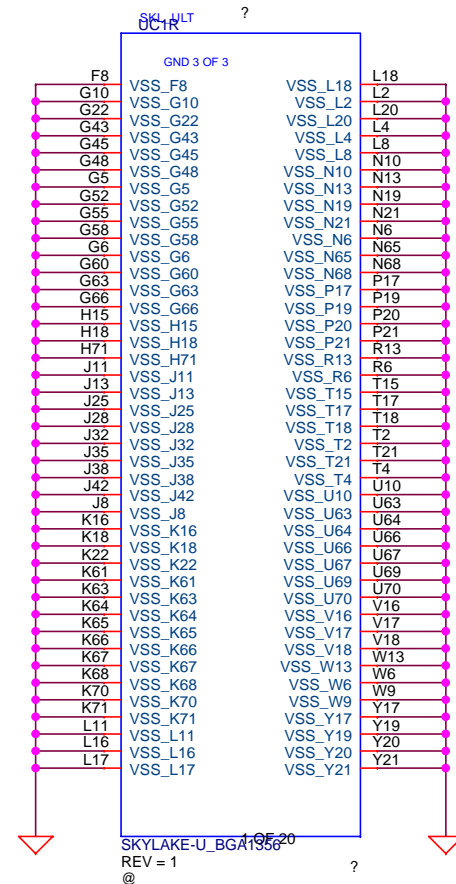
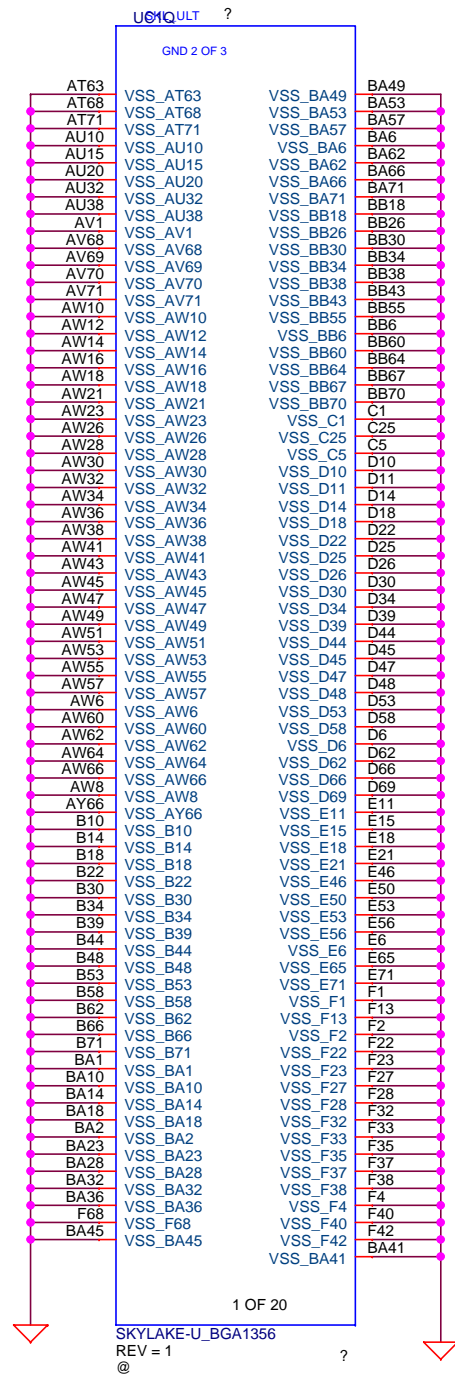
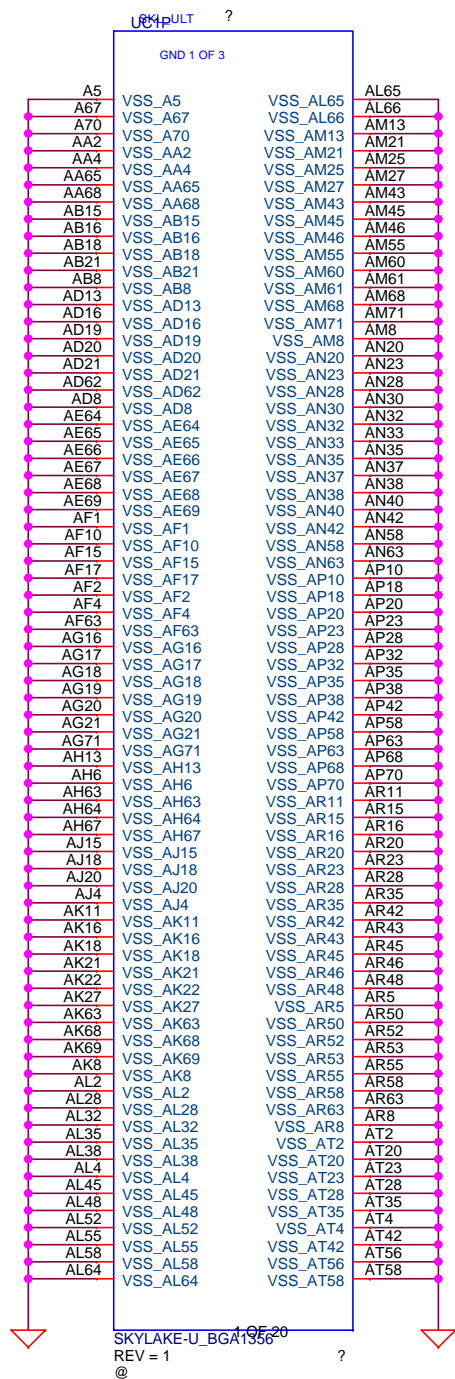
For UMA 2+3e



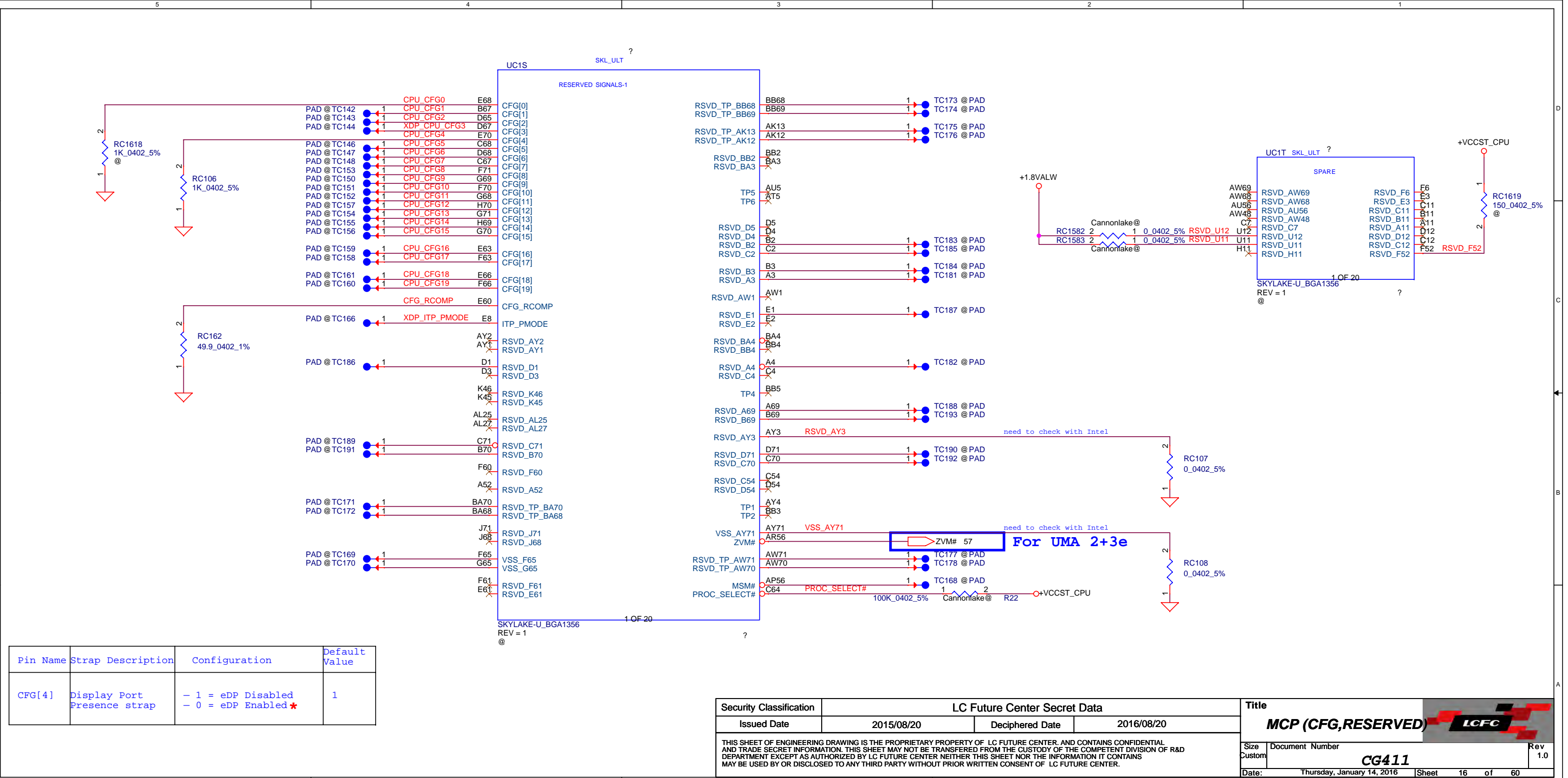
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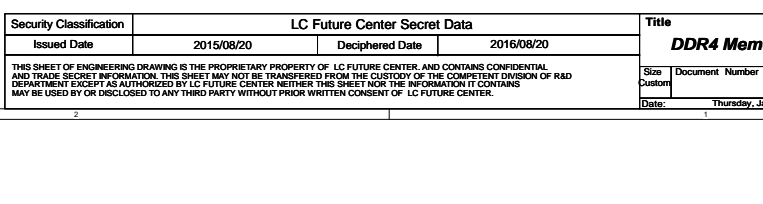
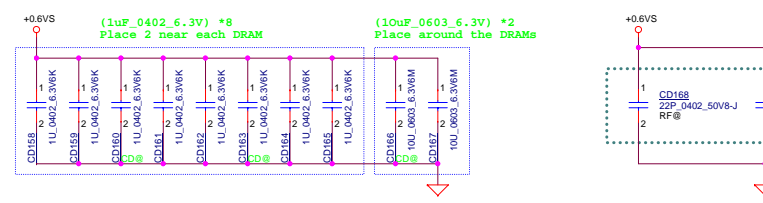
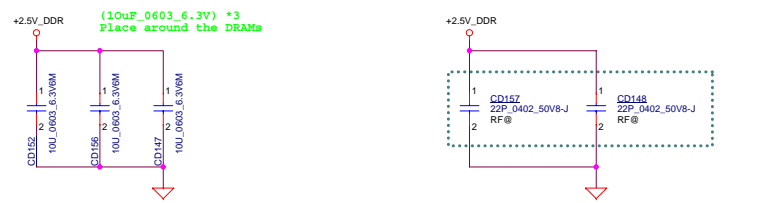
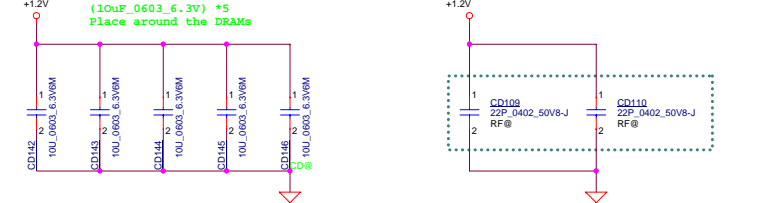
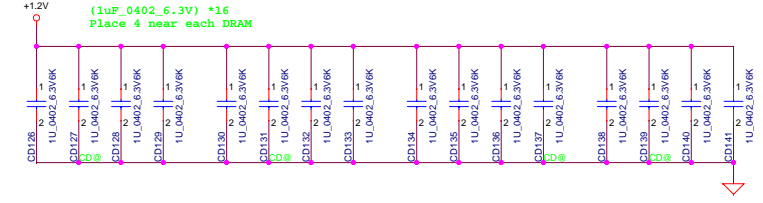
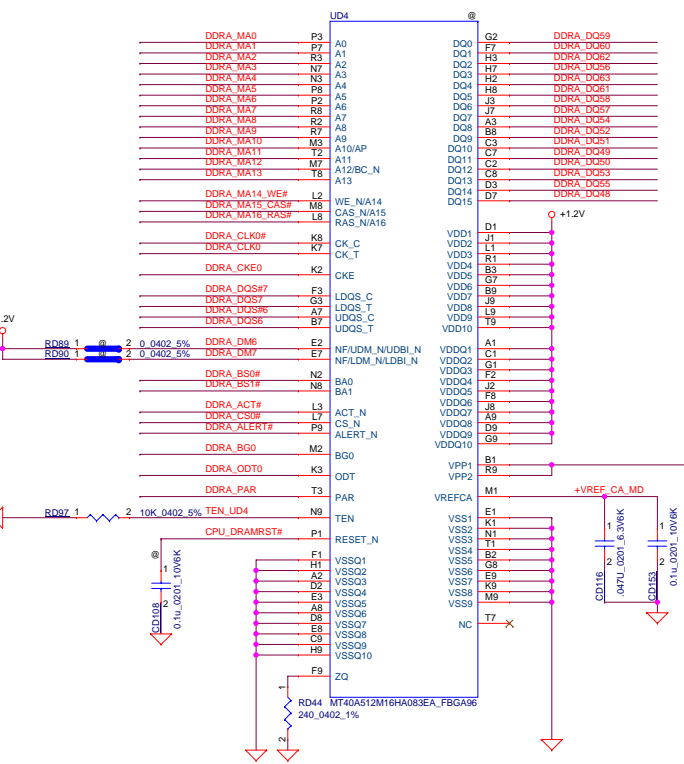
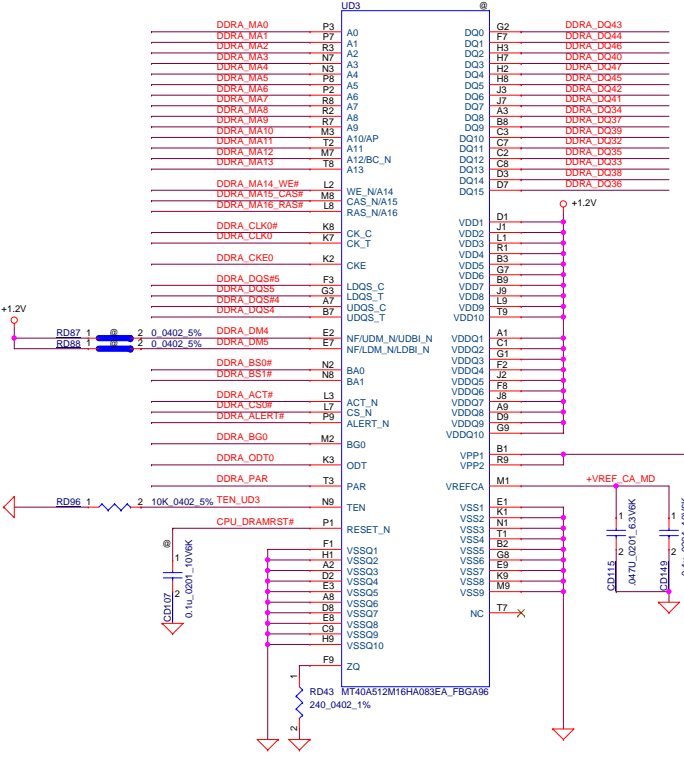
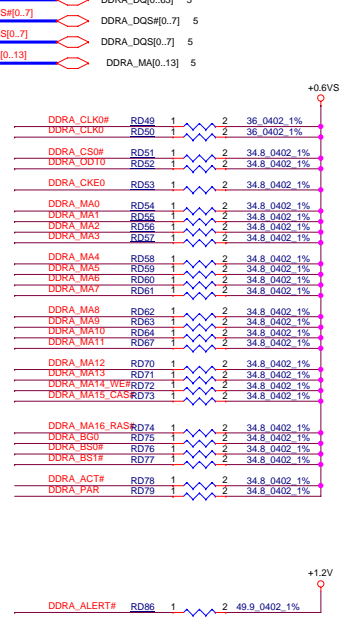
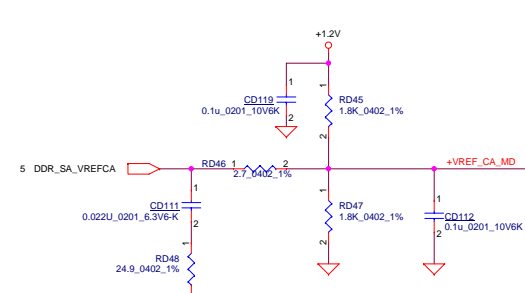
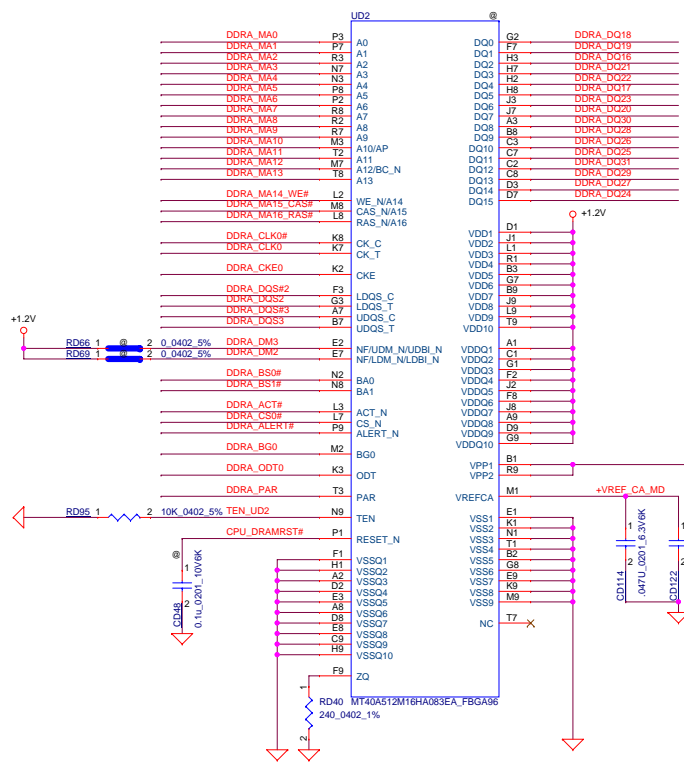
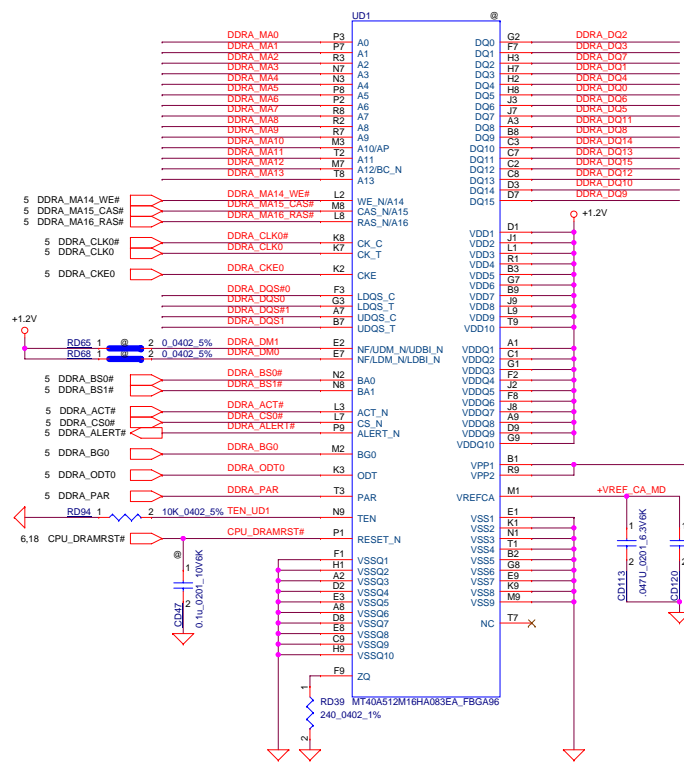


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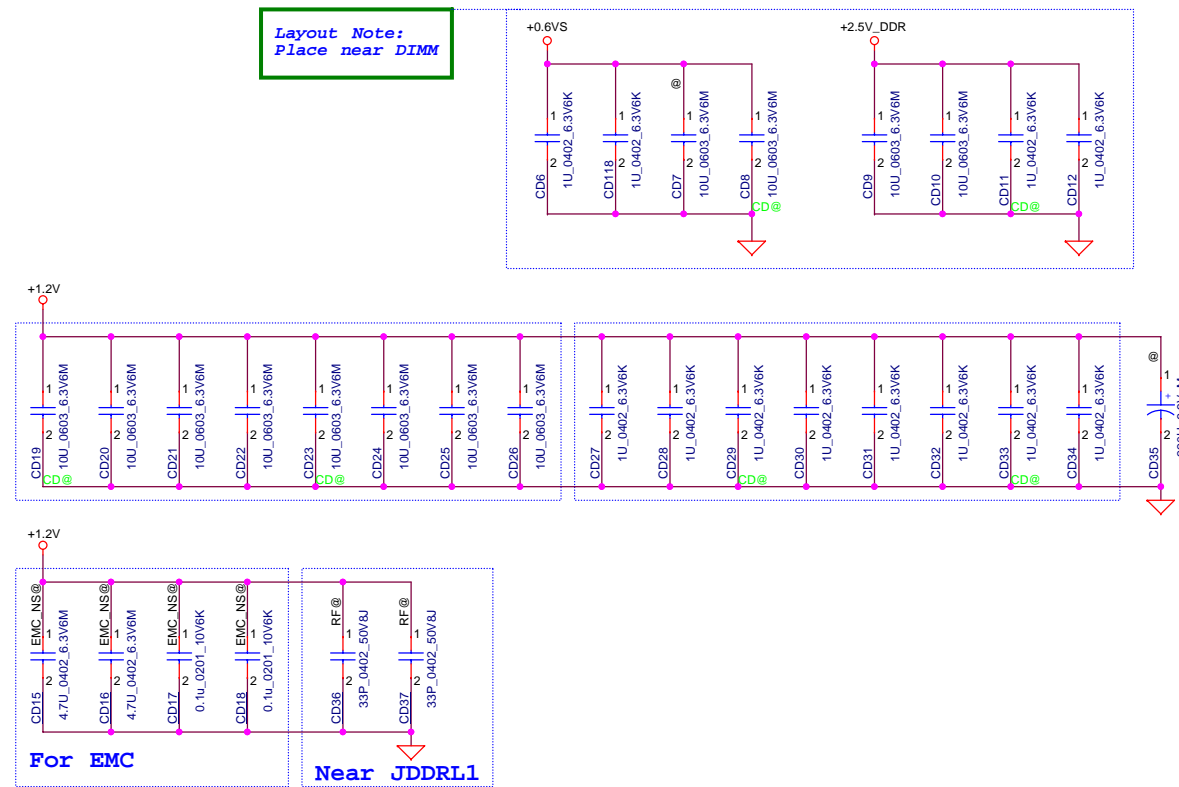
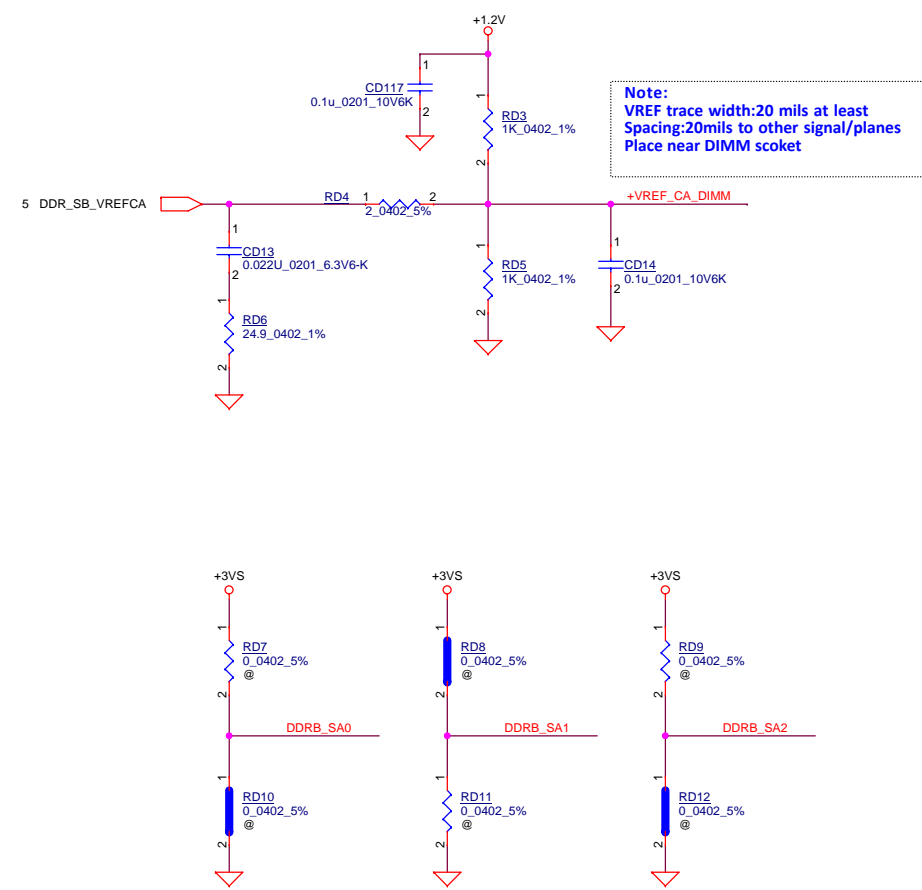
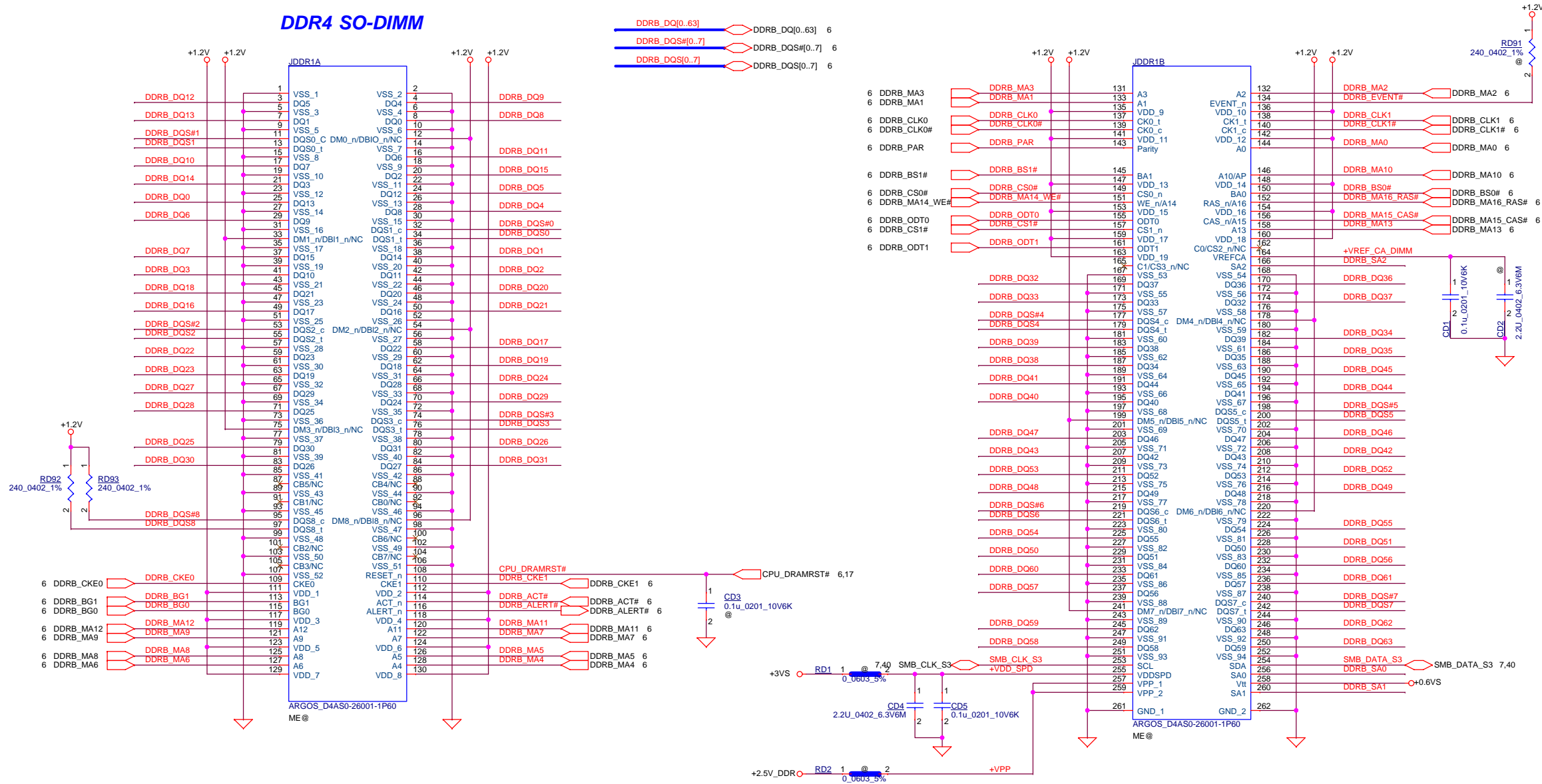
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CFG[4]	Display Port Presence strap	- 1 = eDP Disabled - 0 = eDP Enabled*	1

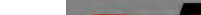




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DDR4 SO-DIMM




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				Date:	Thursday, January 14, 2016	Sheet 22 of 60 Rev 1.0

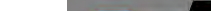
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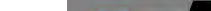
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Security Classification		LC Future Center Secret Data		Title		
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				C	CG411	1.0
				Date:	Thursday, January 14, 2016	Sheet 24 of 60

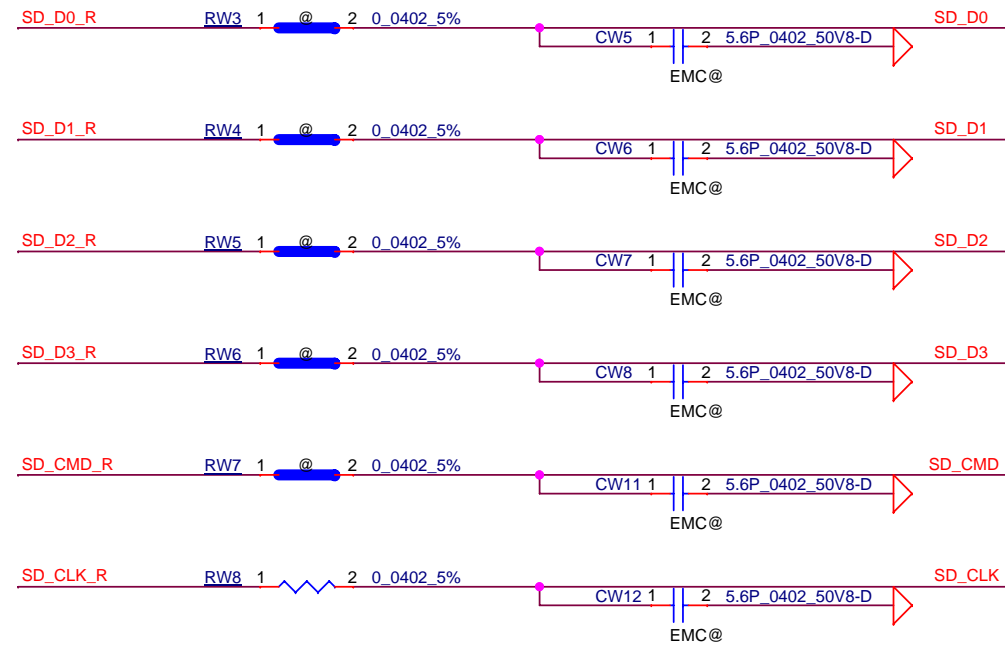
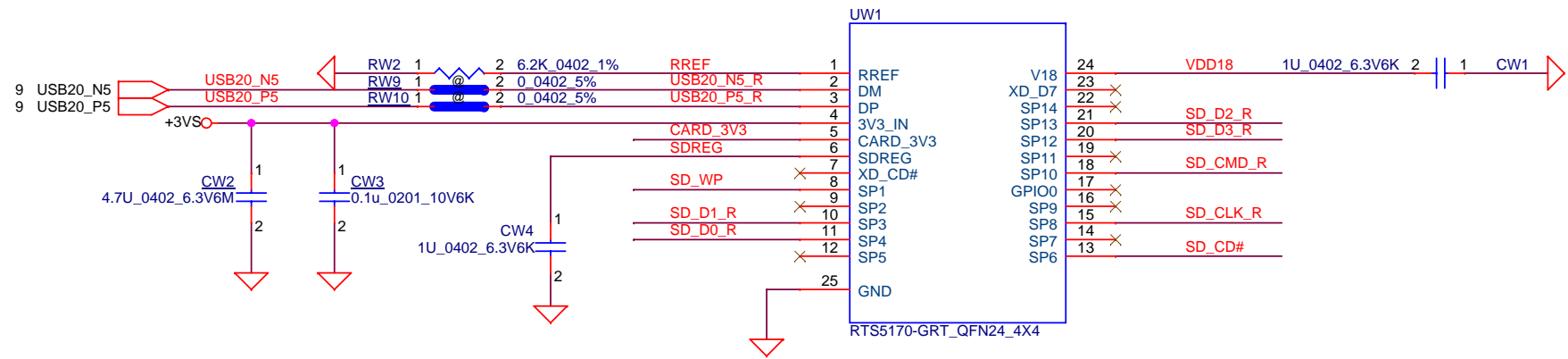
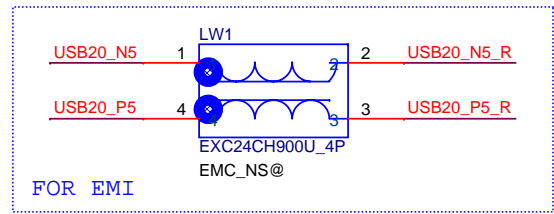
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				CG411		
				Date: Thursday, January 14, 2016		Sheet 25 of 60

Security Classification		LC Future Center Secret Data		Title		
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				C	CG411	1.0
Date:				Thursday, January 14, 2016	Sheet	26 of 60

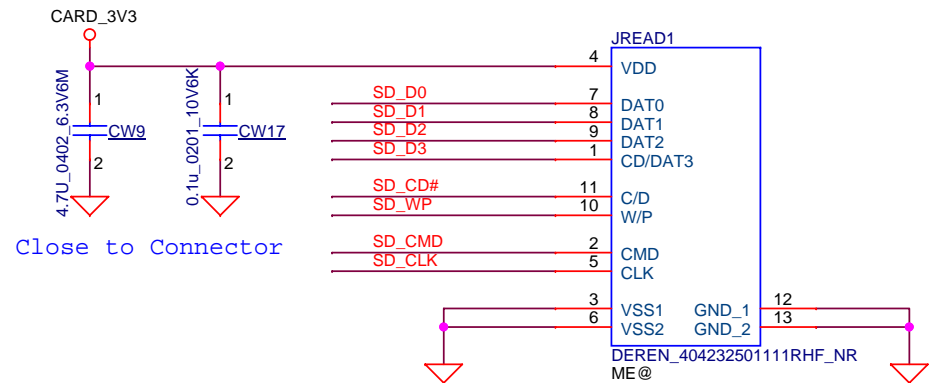
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		2		Date: Thursday, January 14, 2016		Sheet 27 of 60

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				Date:	Thursday, January 14, 2016	Sheet 28 of 60 Rev 1.0

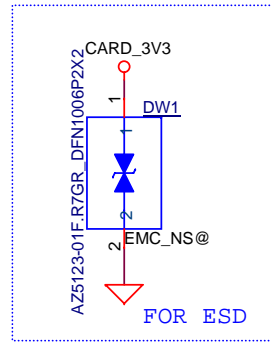
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A																								
5					4					3					2					1				



SD / MMC




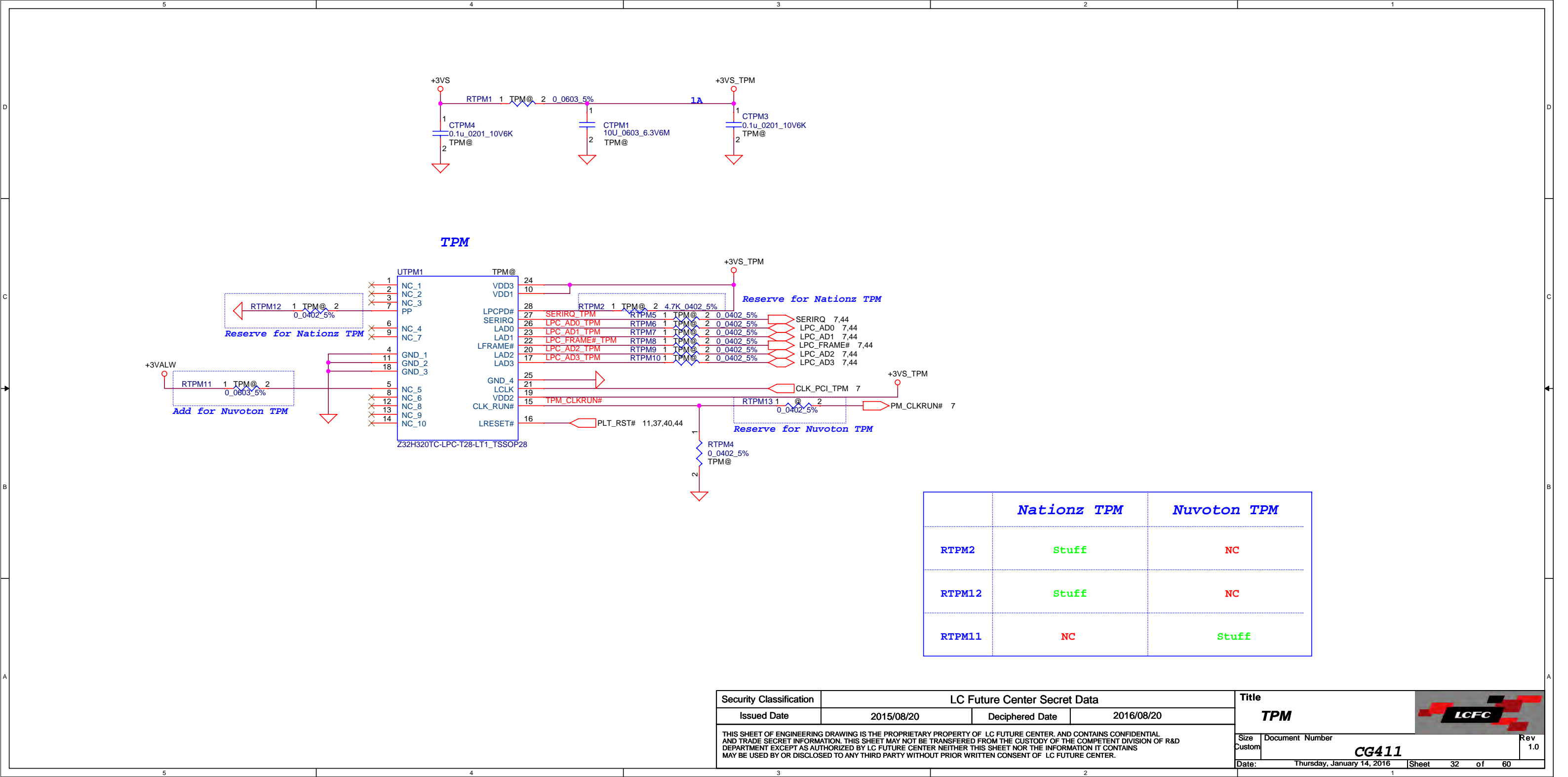
Close to Connector



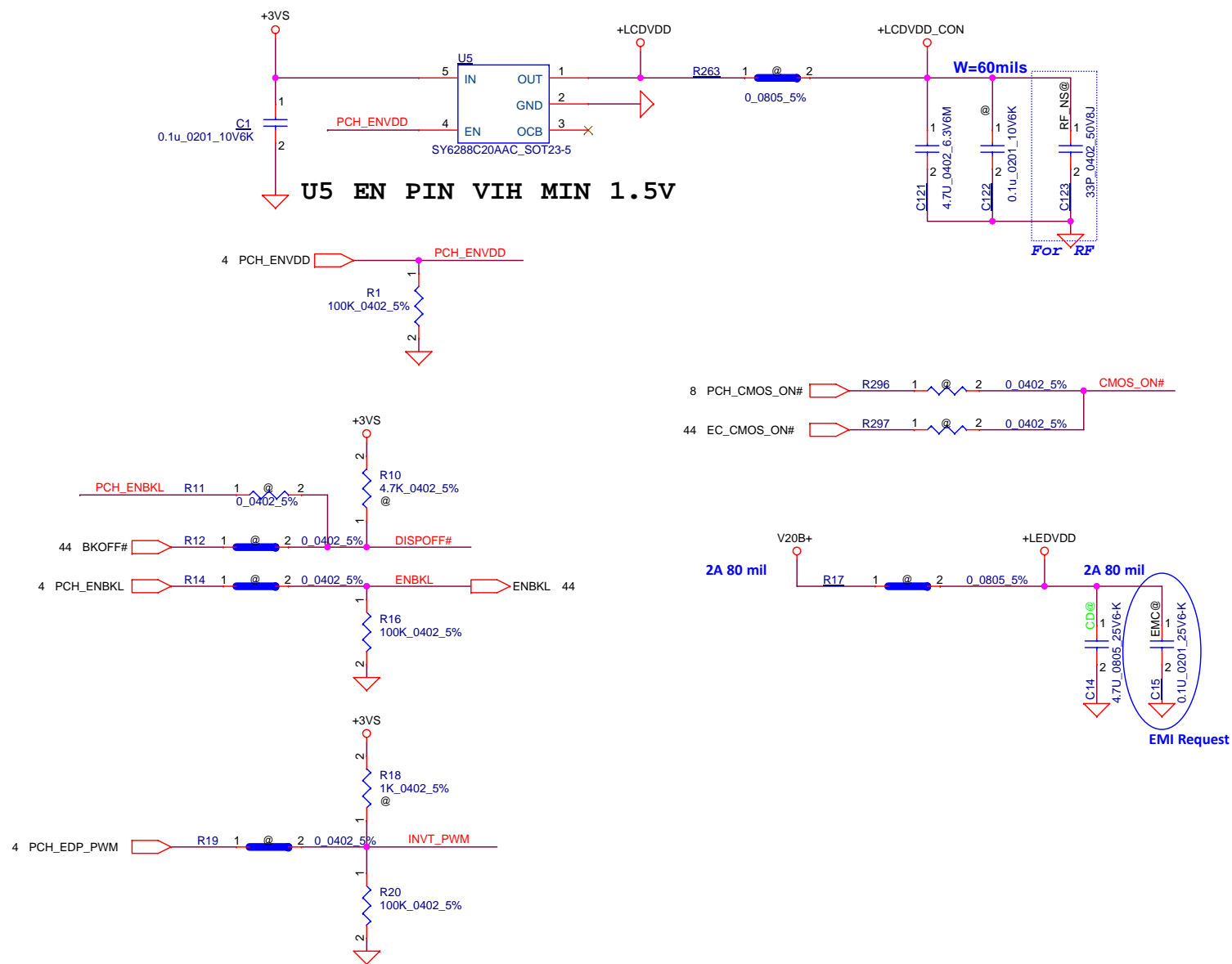
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				Date:	Thursday, January 14, 2016
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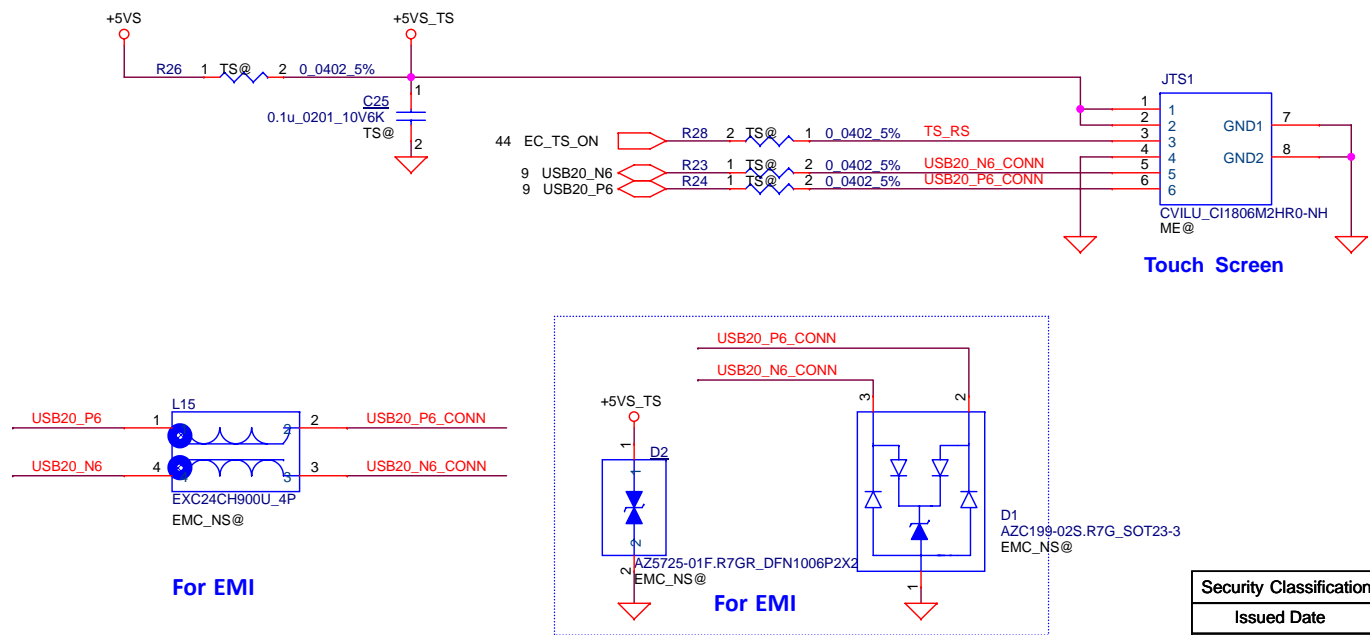
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				Custom	CG411	1.0
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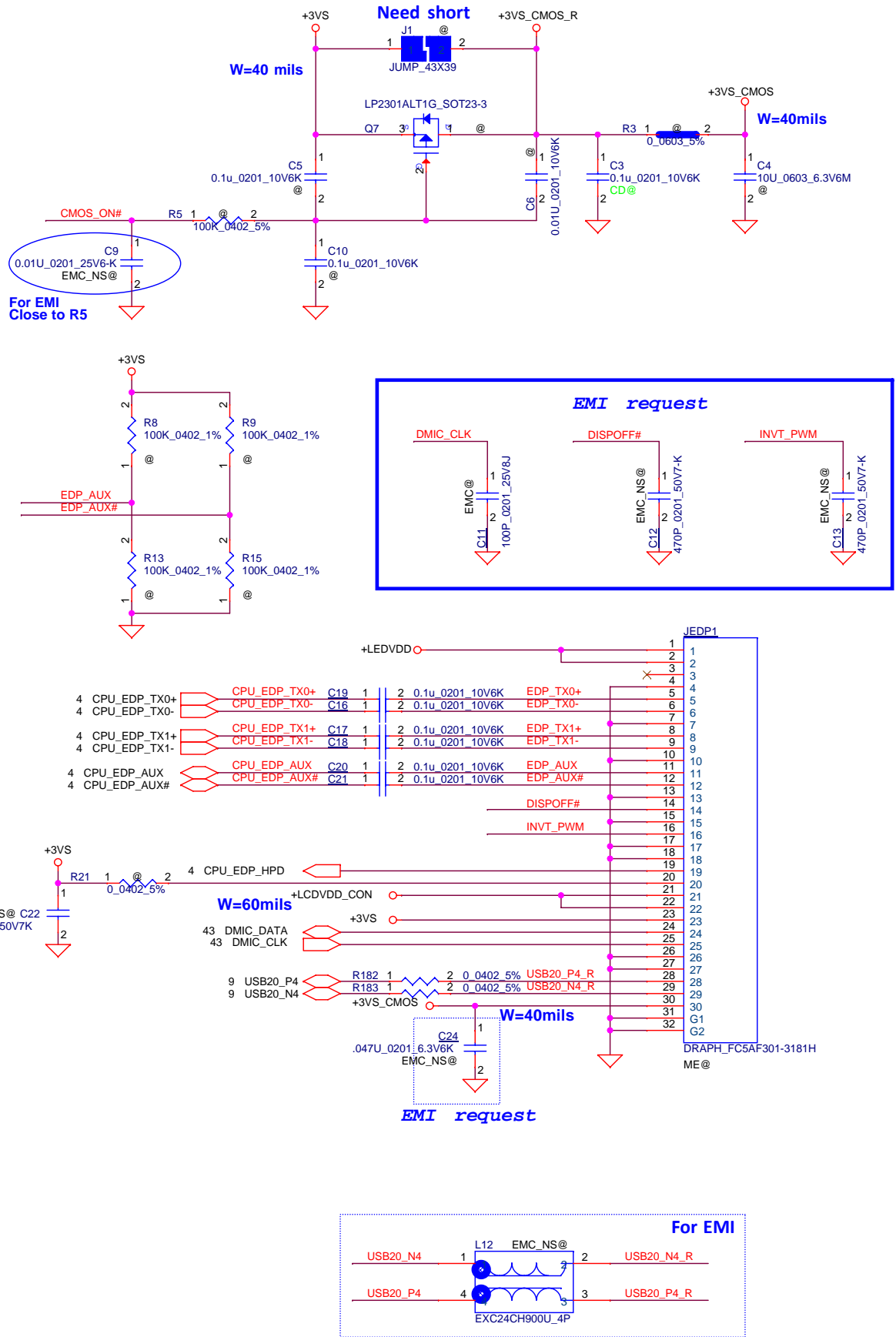
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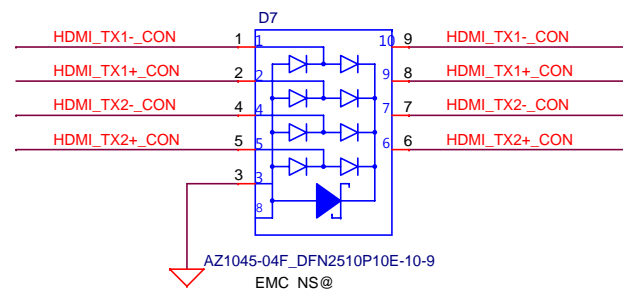
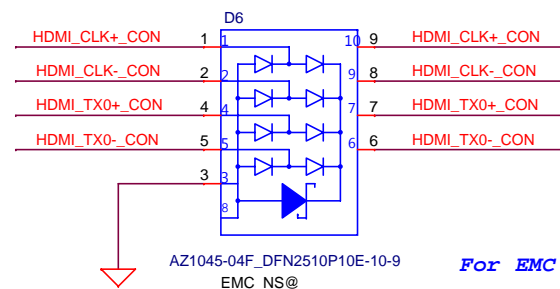
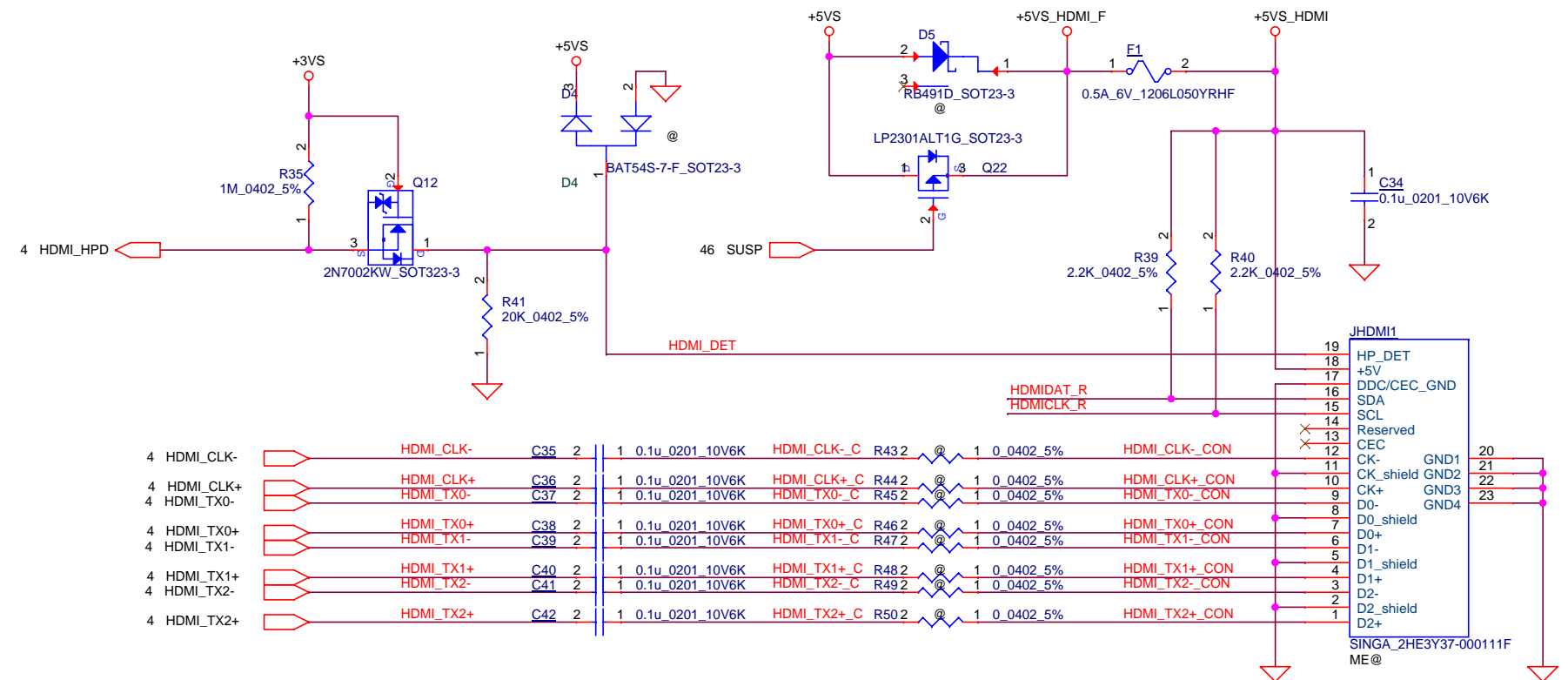
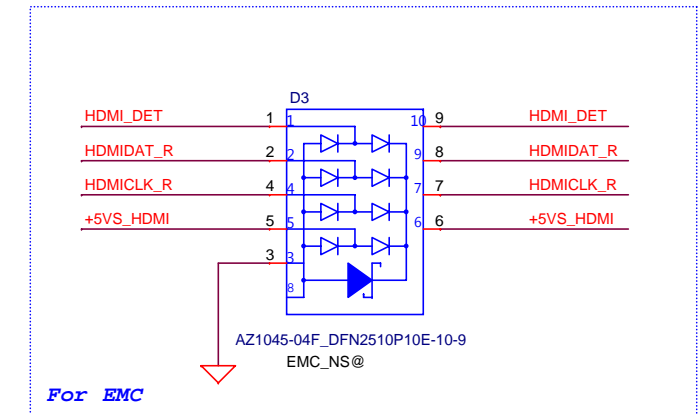
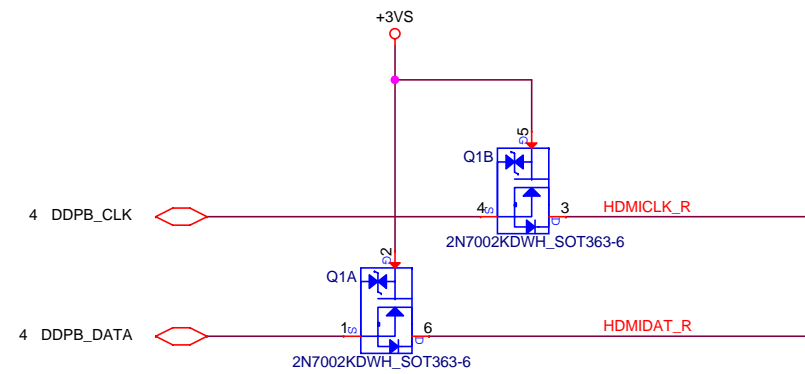
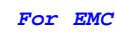



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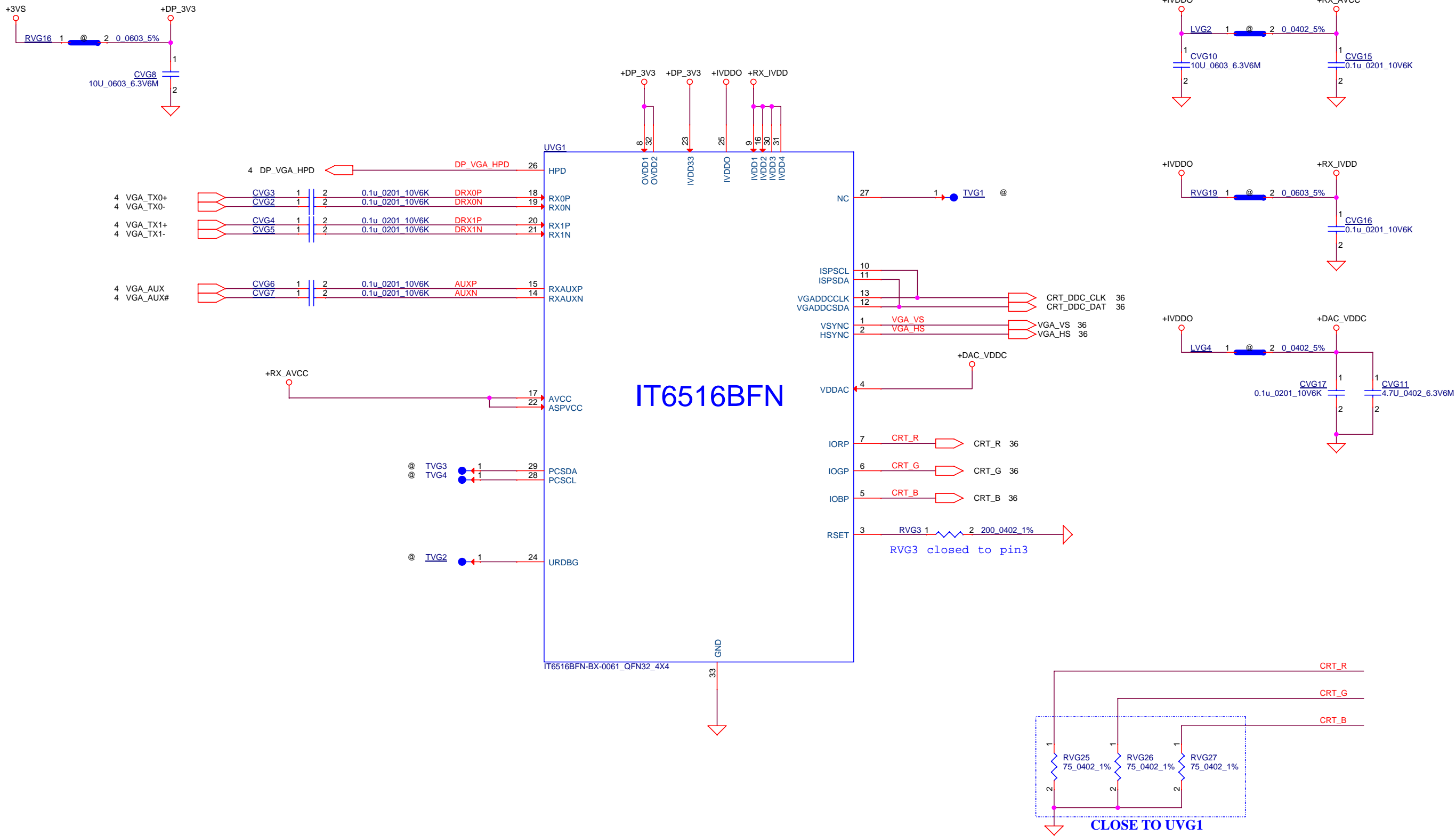


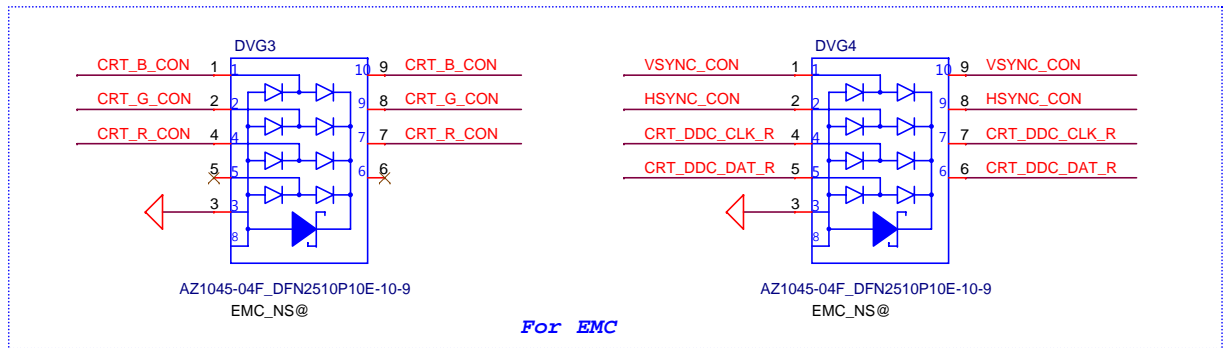
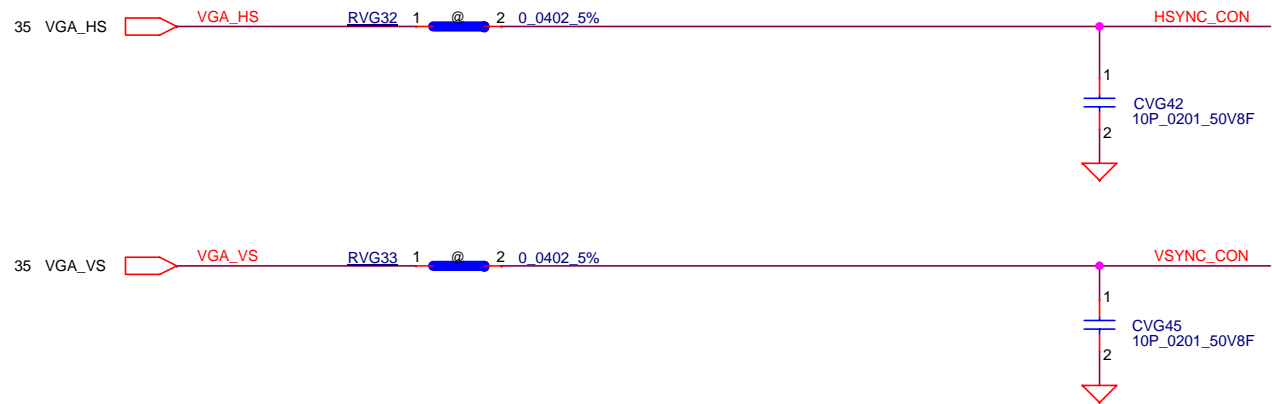
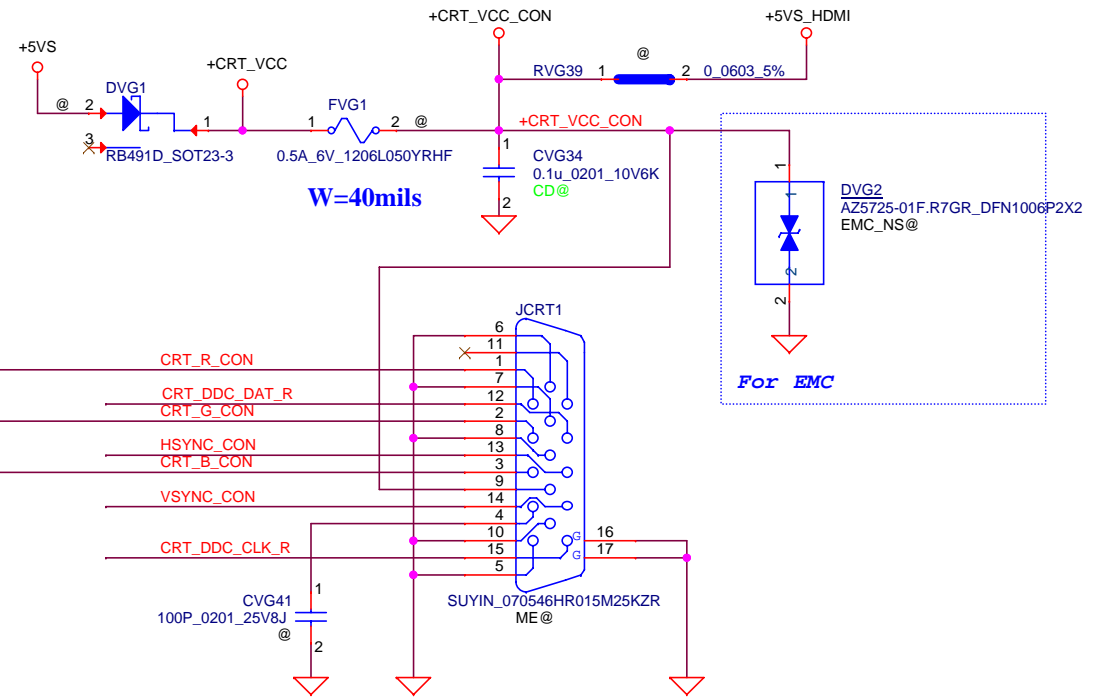
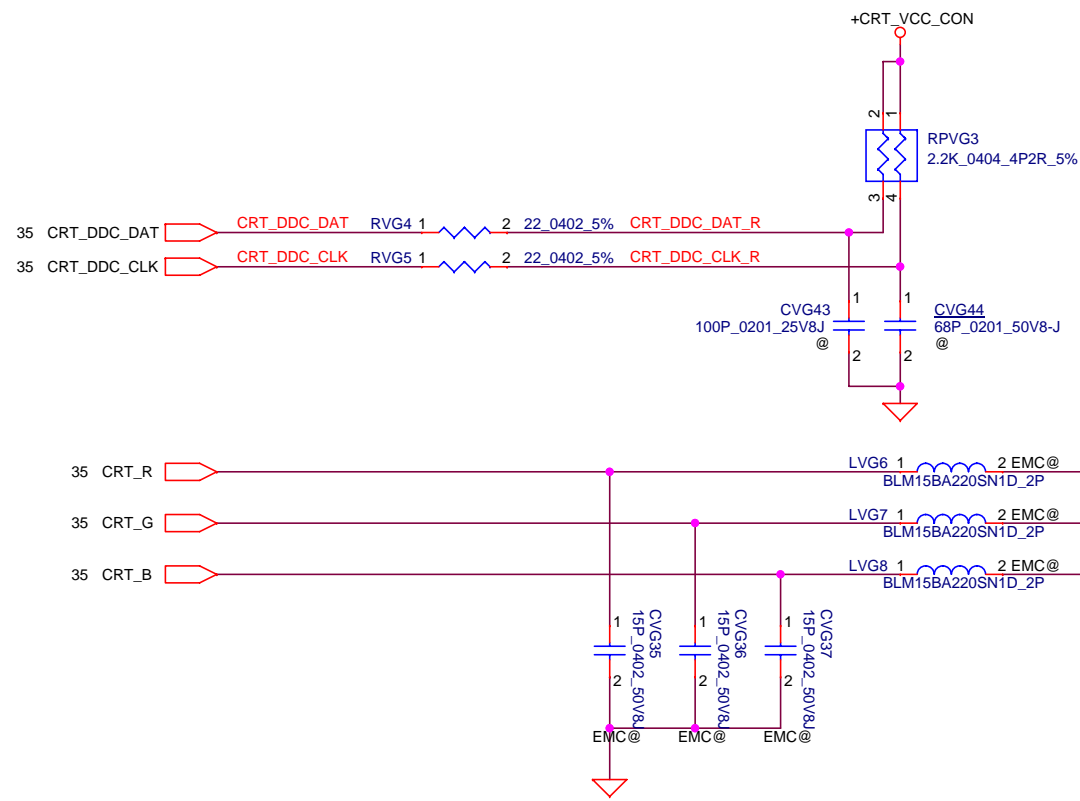
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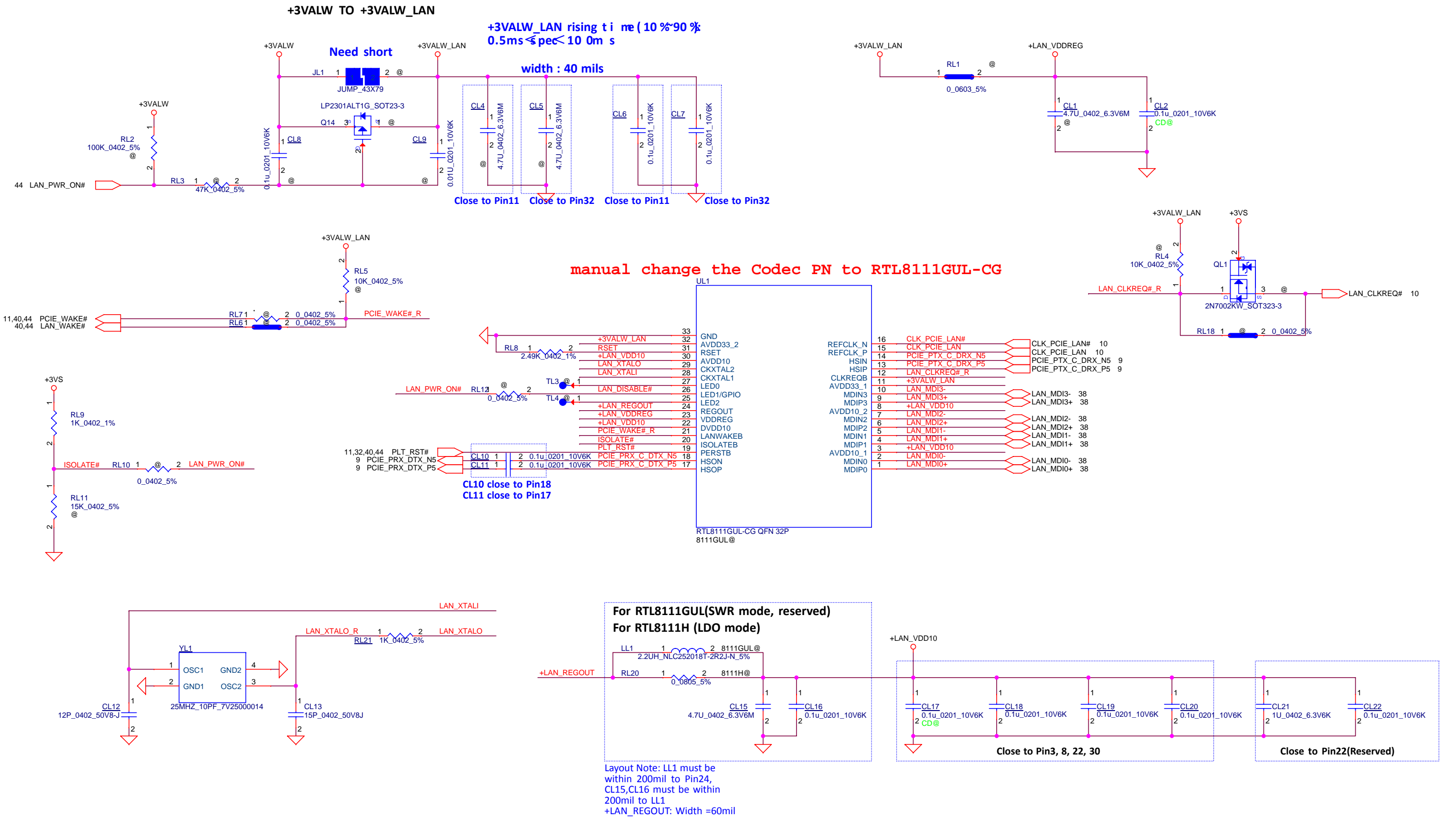



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				Custom	CG411		1.0
				Date:	Thursday, January 14, 2016		Sheet 34 of 60



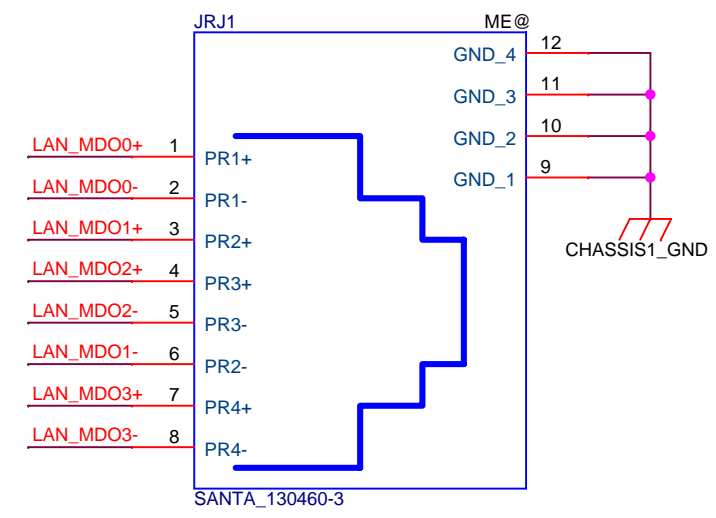
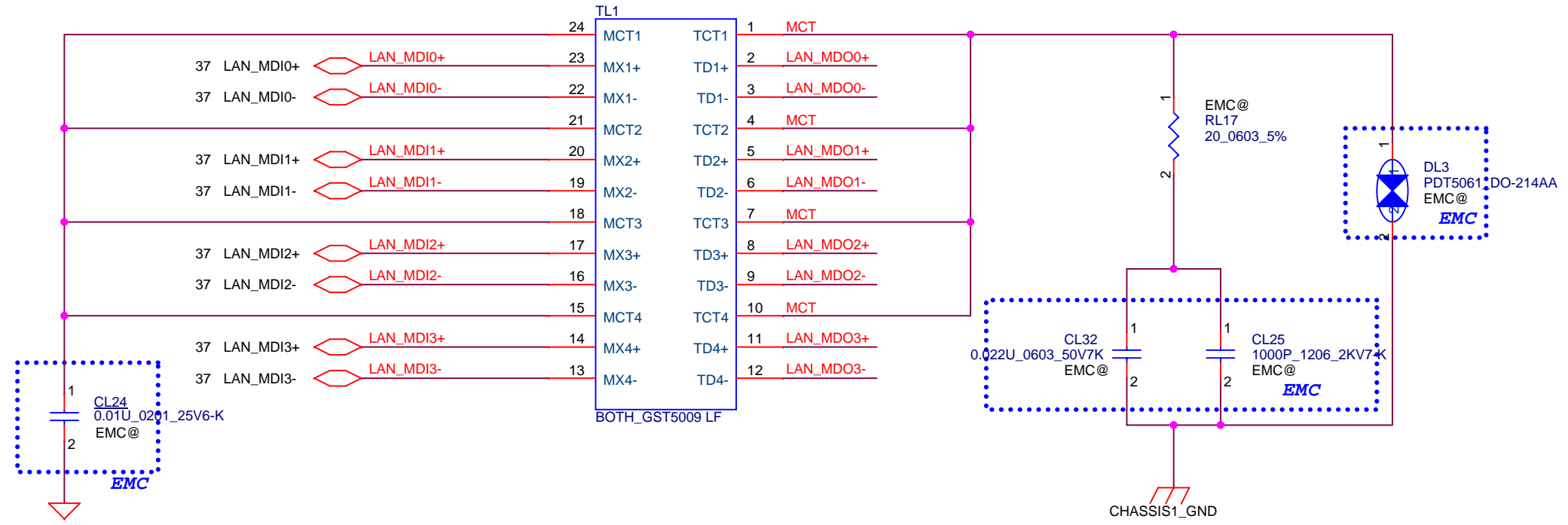
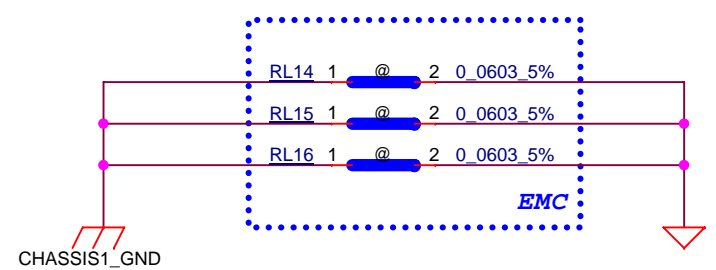
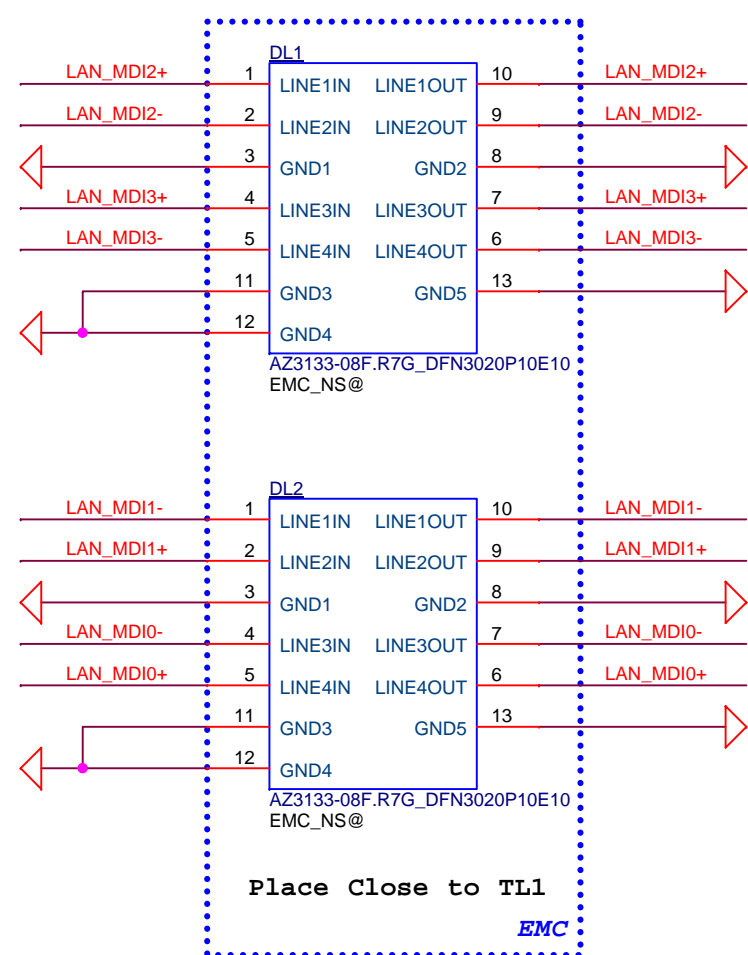



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				Date:	Thursday, January 14, 2016	Sheet 36 of 60

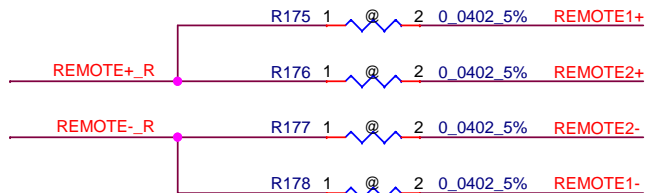
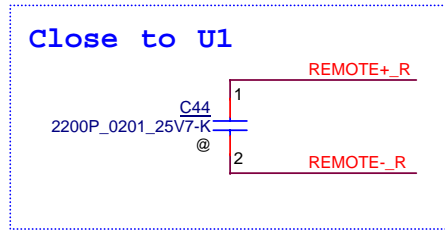


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					Document Number CG411
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Date: Thursday, January 14, 2016					Sheet 37 of 60

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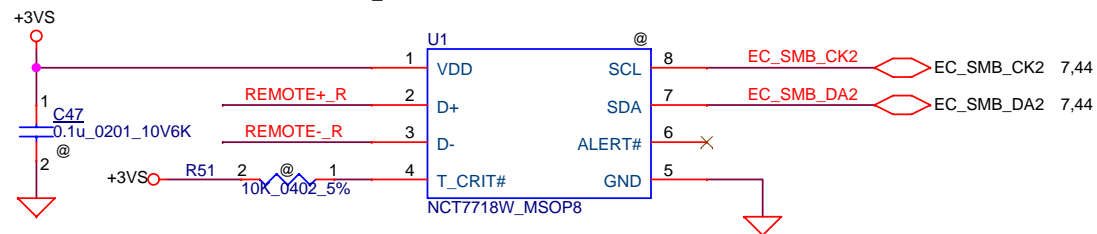


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Size		Document Number								Rev	
B		CG411								1.0	
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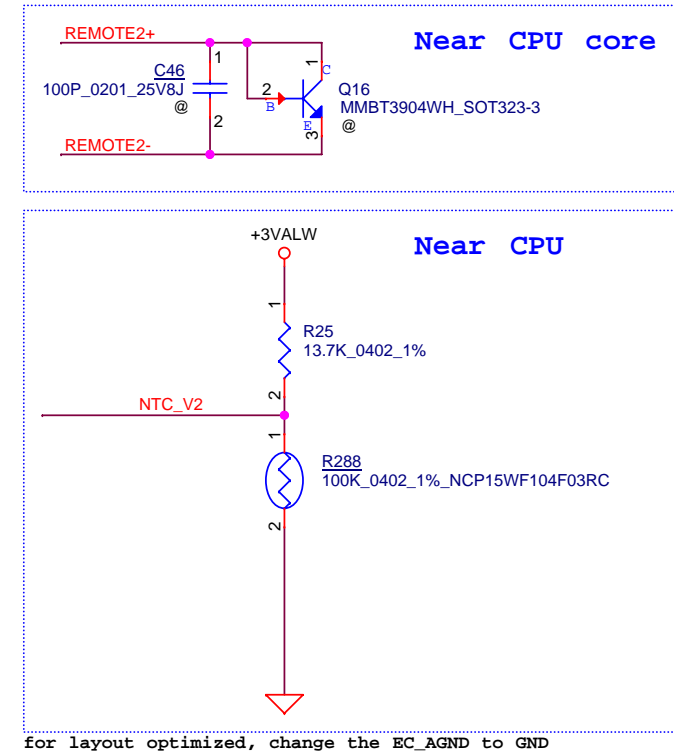
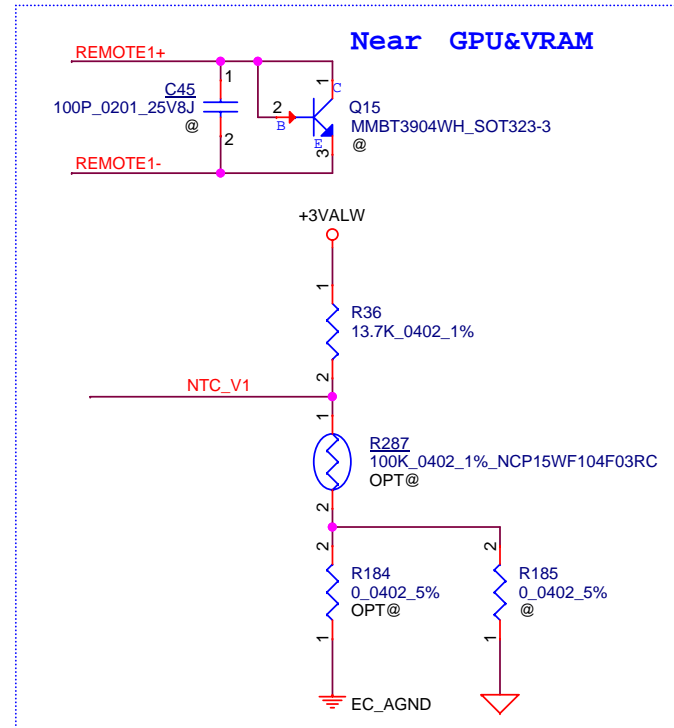


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Trace length:<8"

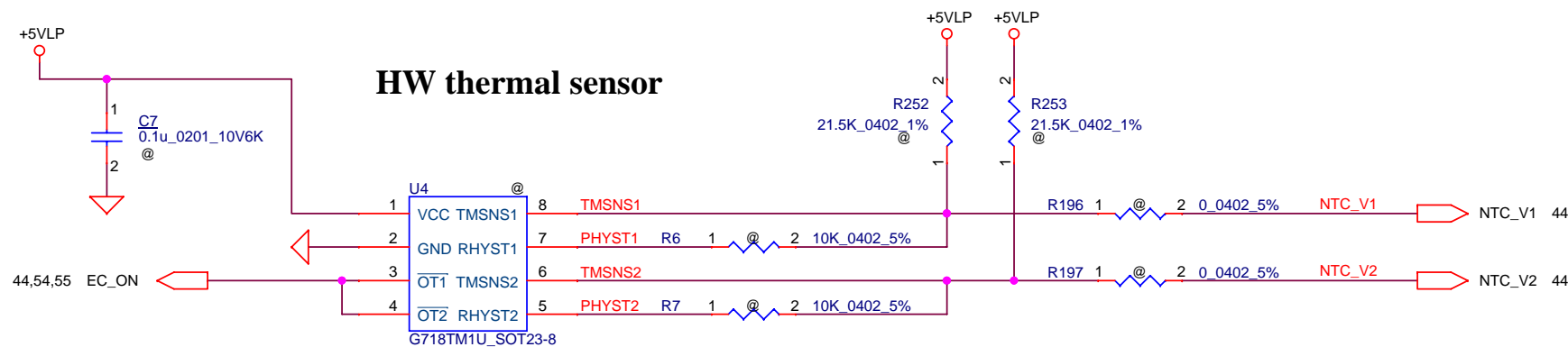
SMSC thermal sensor placed near DIMM



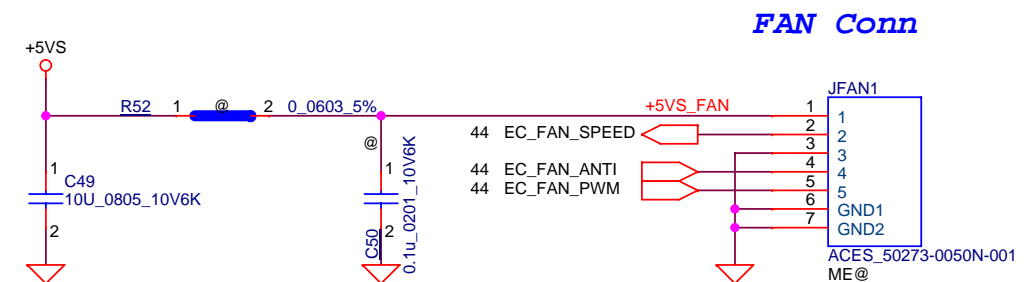
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HW thermal sensor

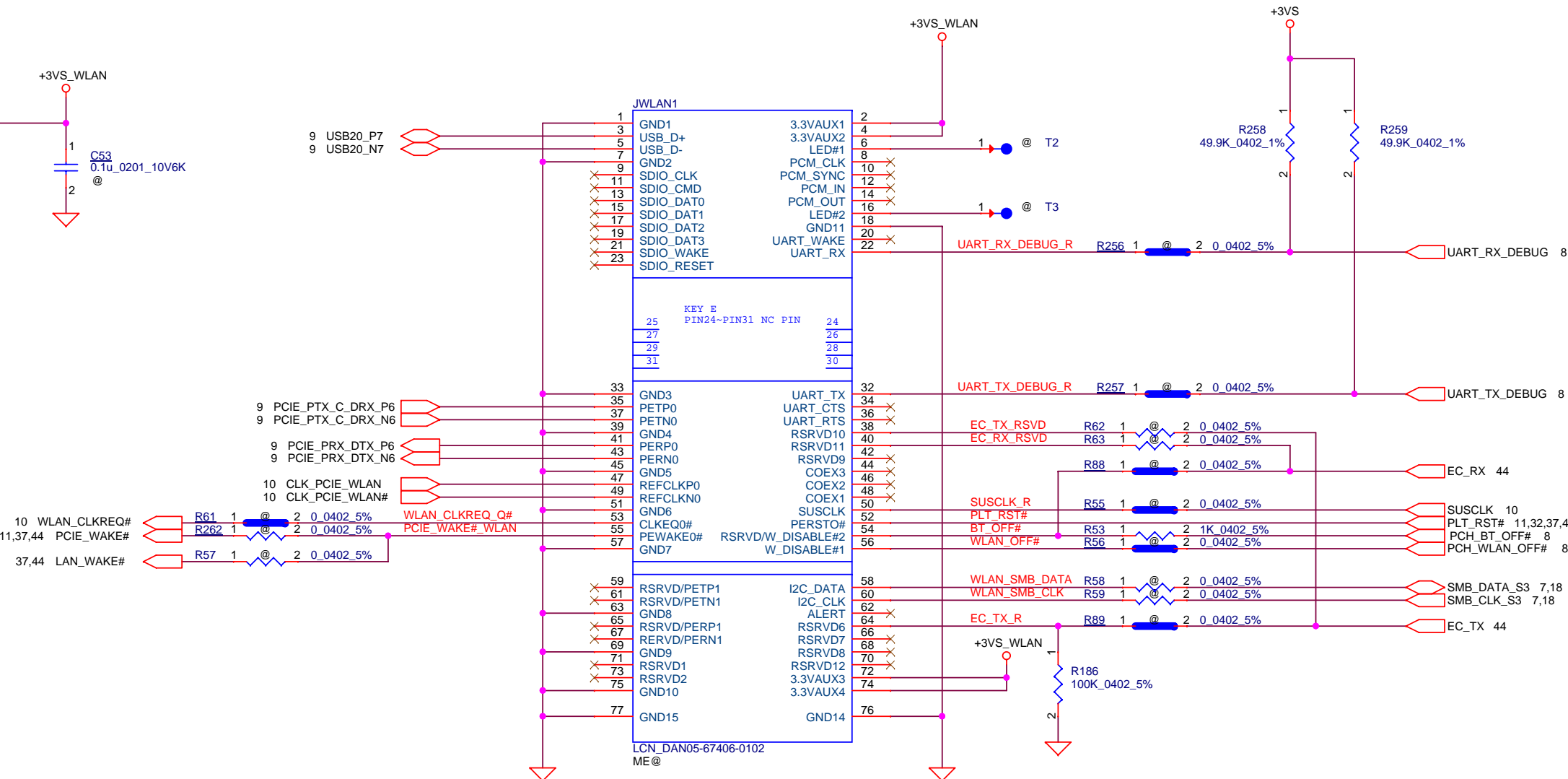


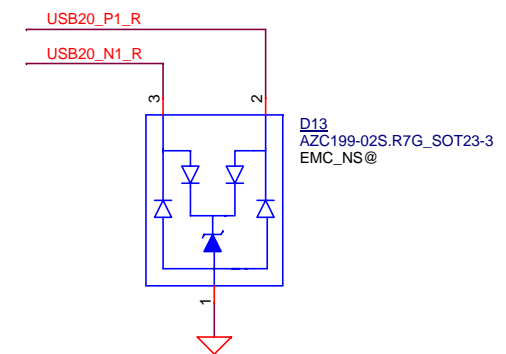
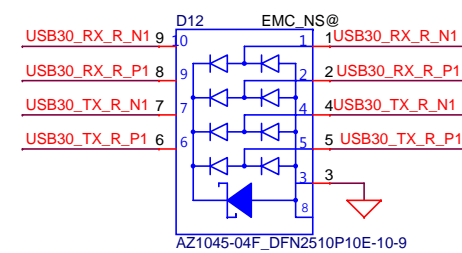
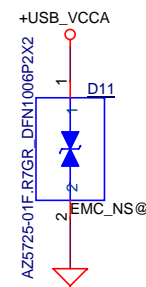
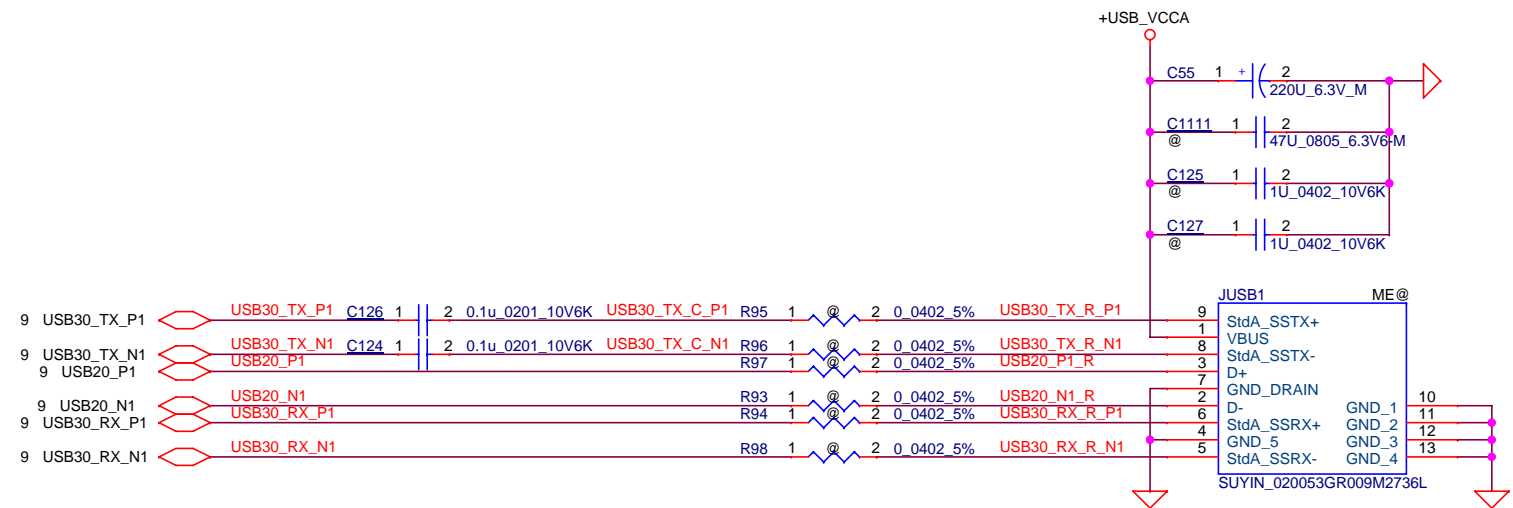
over temperature threshold:
 $RSET=3*RTMH$
92+/-30C
Hysteresis temperature threshold.
 $RHYST=(RSET*RTML)/(3*RTML-RSET)$
56+/-30C




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					CG411	
Date:		Thursday, January 14, 2016		Sheet	39 of 60	1

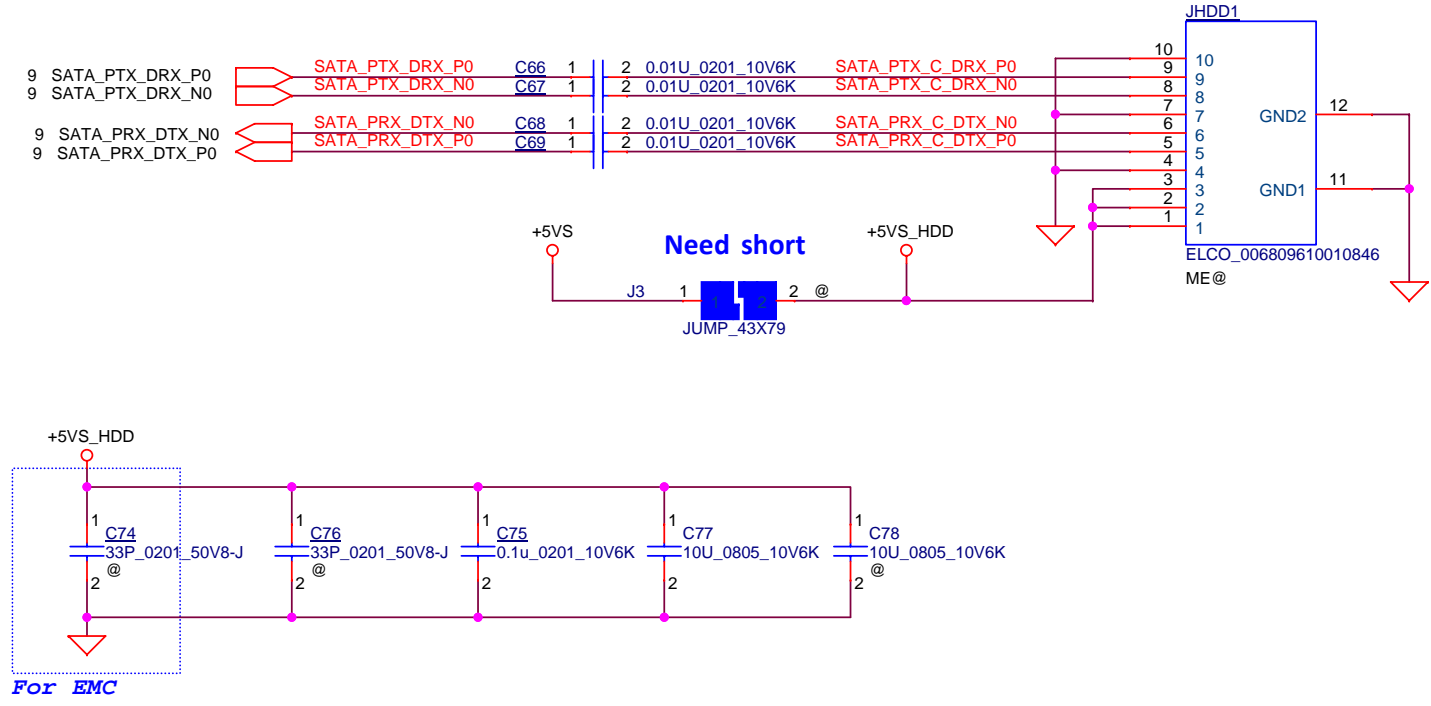
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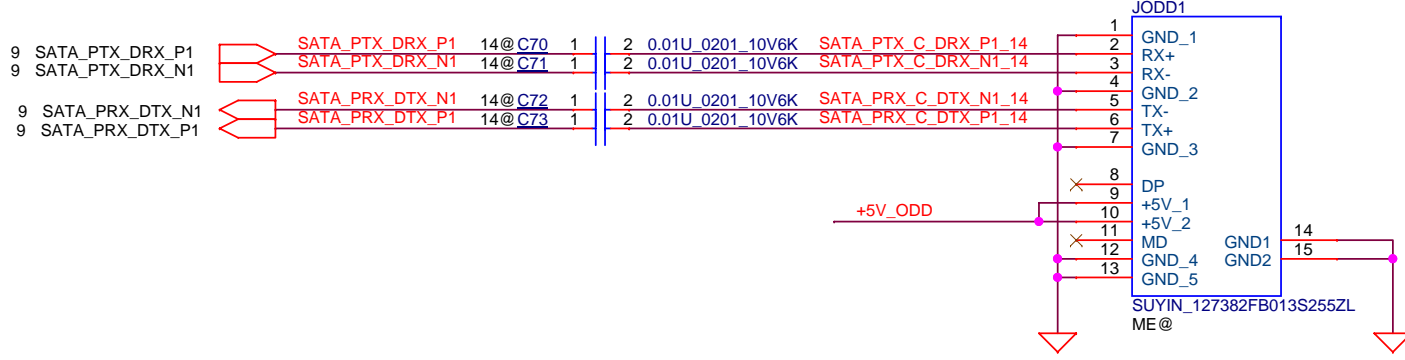


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				Custom	CG411	1.0
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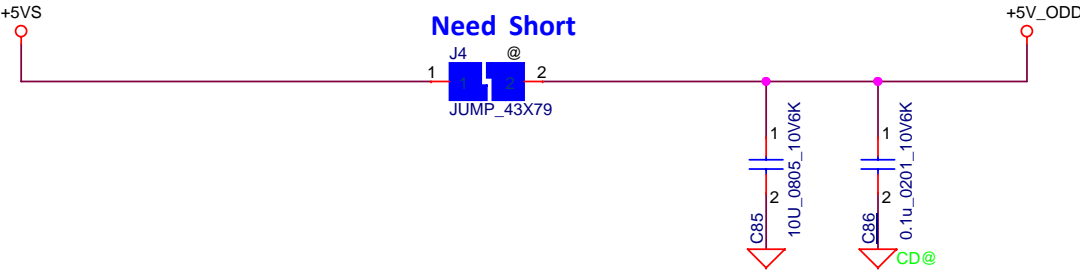
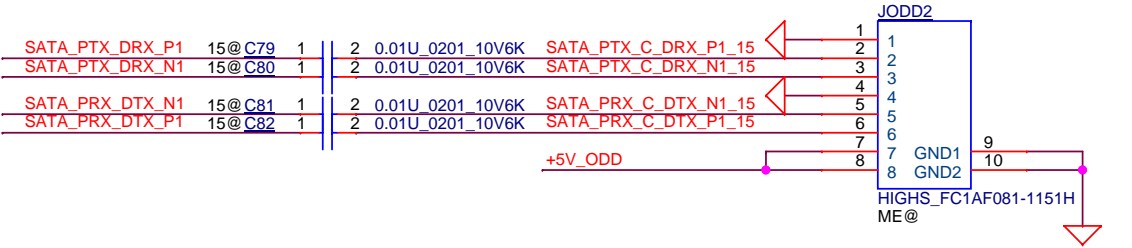
SATA HDD Conn.




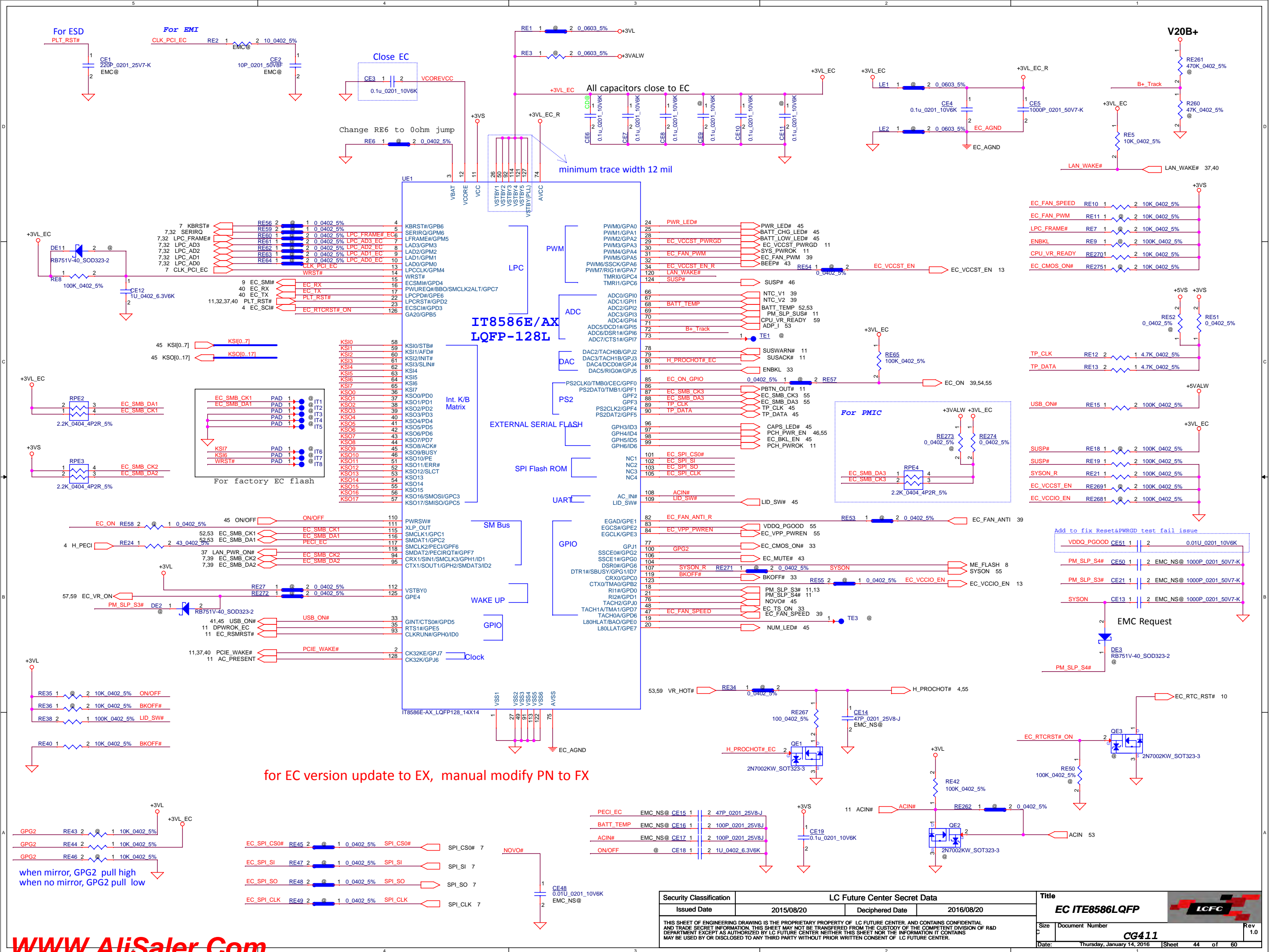
FOR 14" SATA ODD Conn.



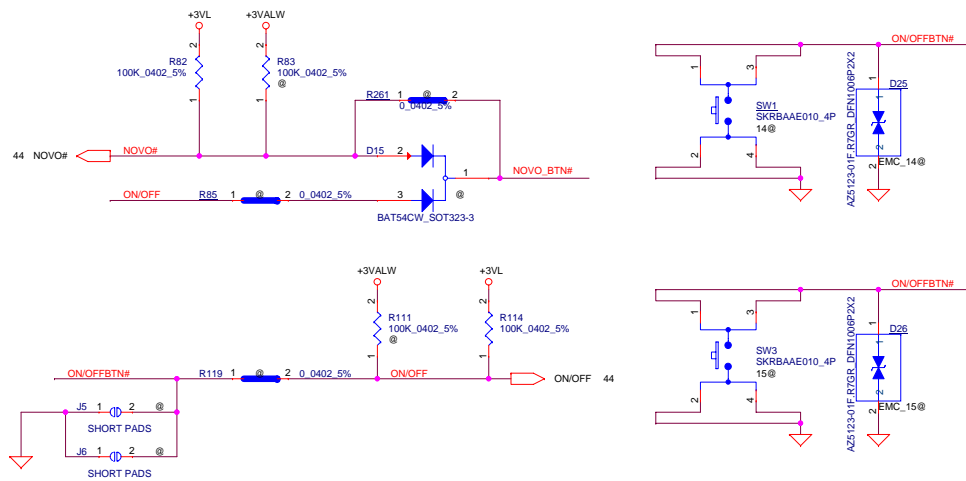
FOR 15" SATA ODD FFC Conn



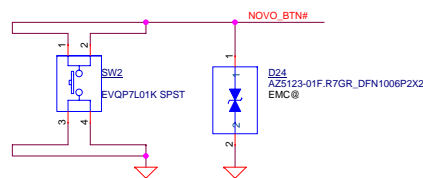
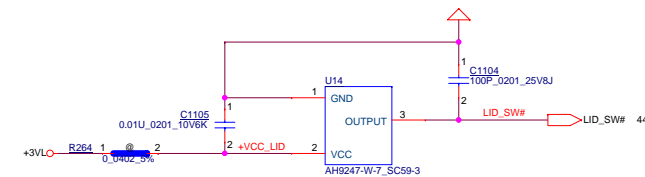
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Issued Date	2015/08/20	Deciphered Date	2016/08/20	HDD/ODD CONN		
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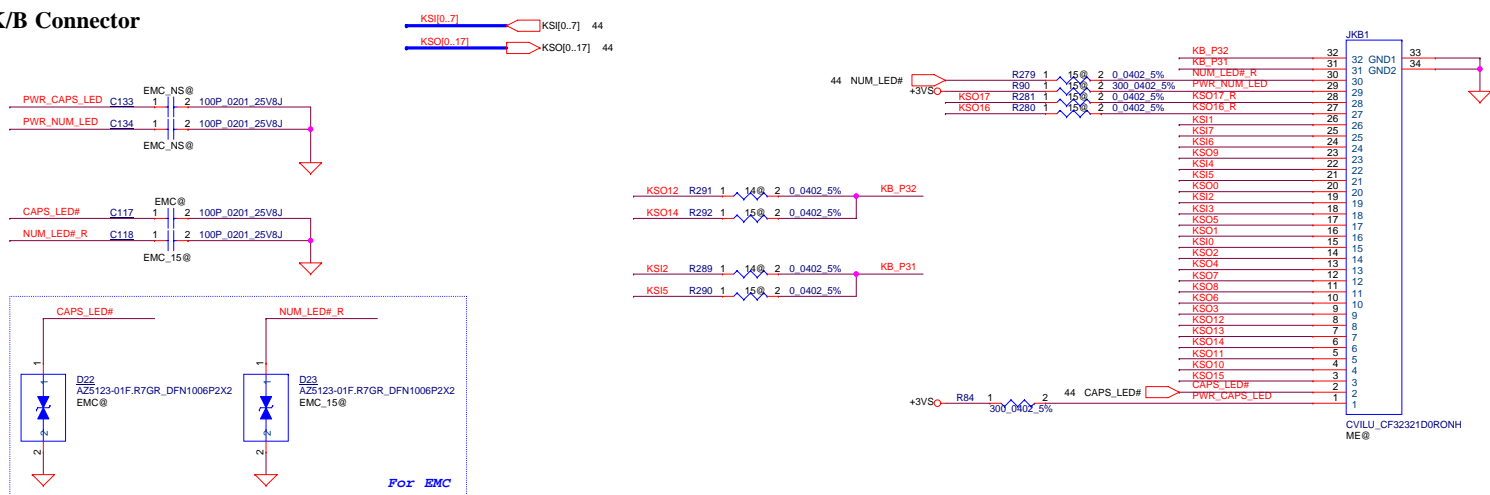
ON/OFF switch



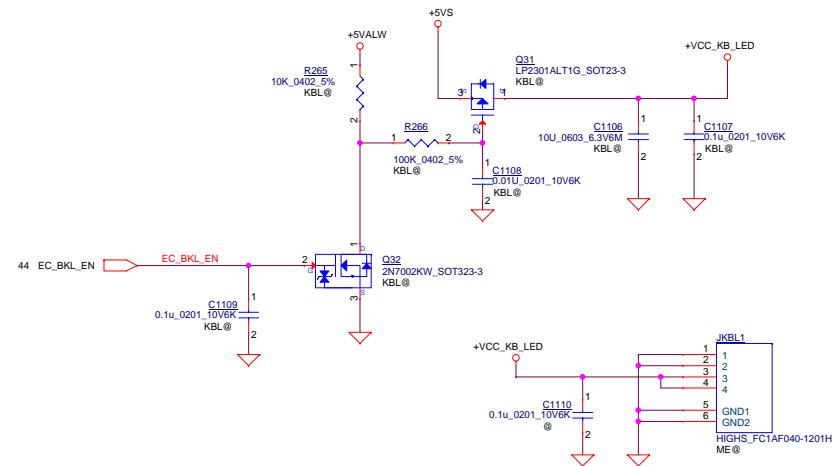
Novo button

**LID switch**

K/B Connector

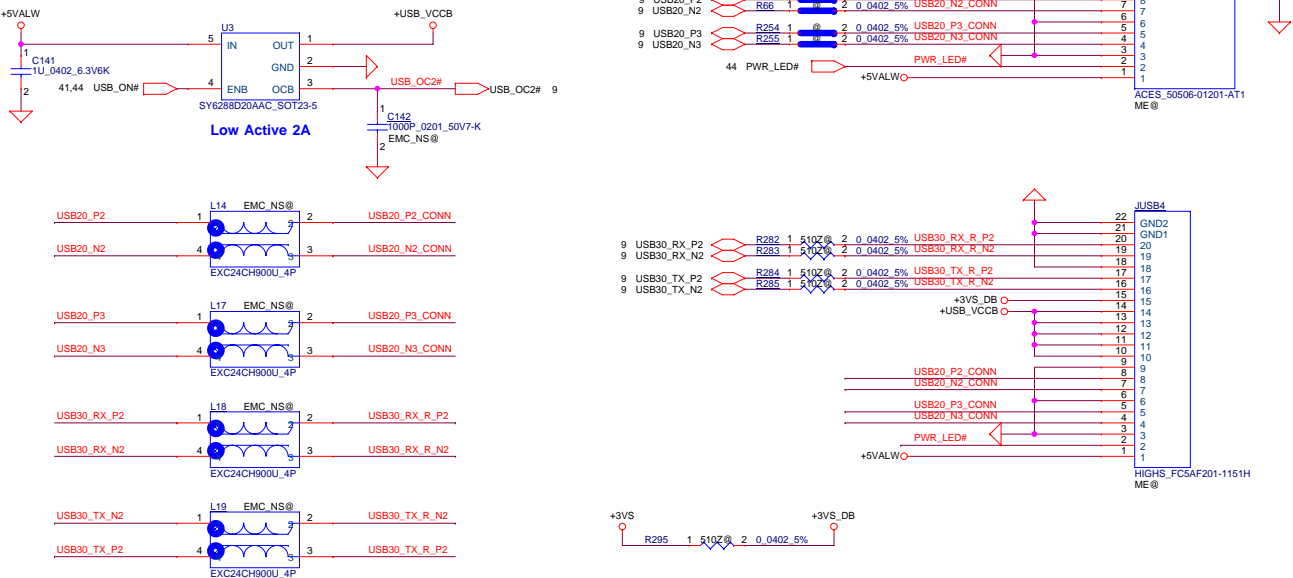


KB Backlight Connector

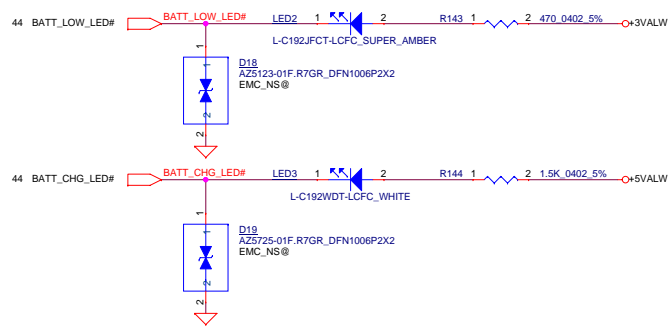
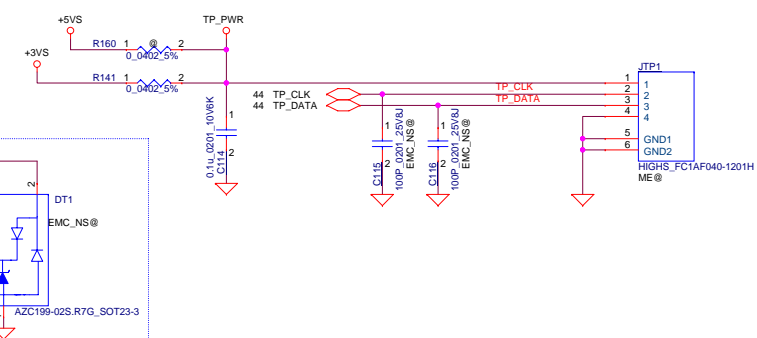


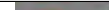
USB DB Connector

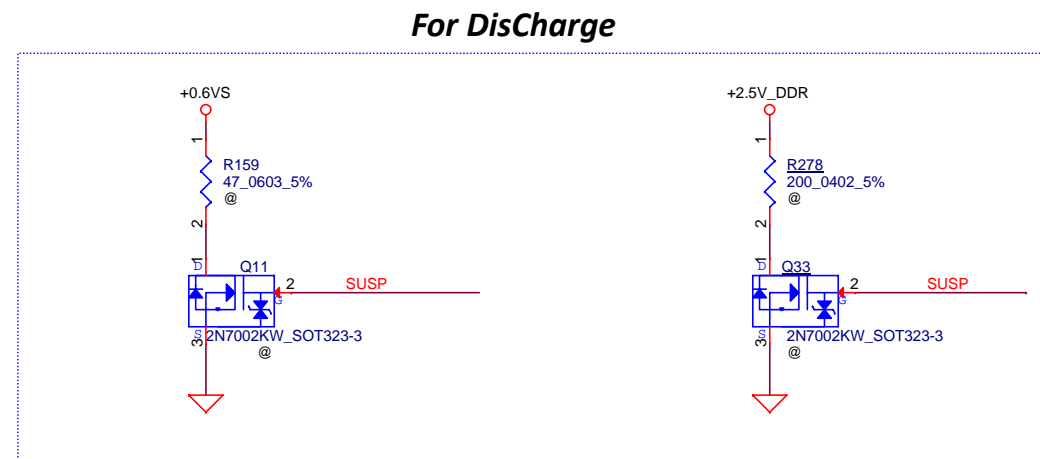
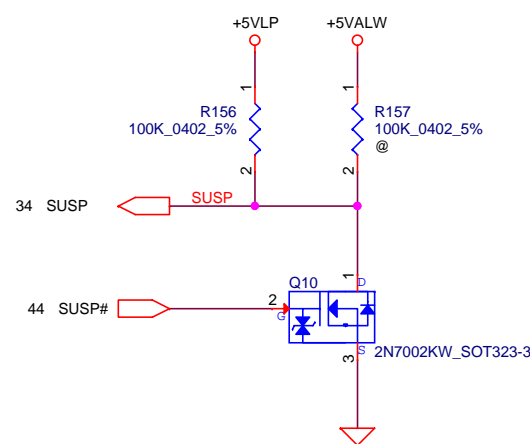
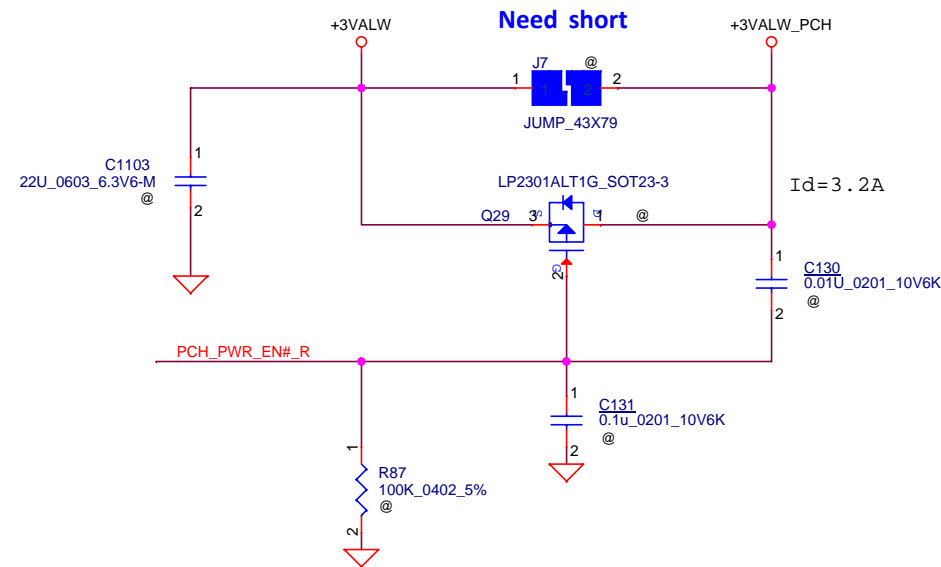
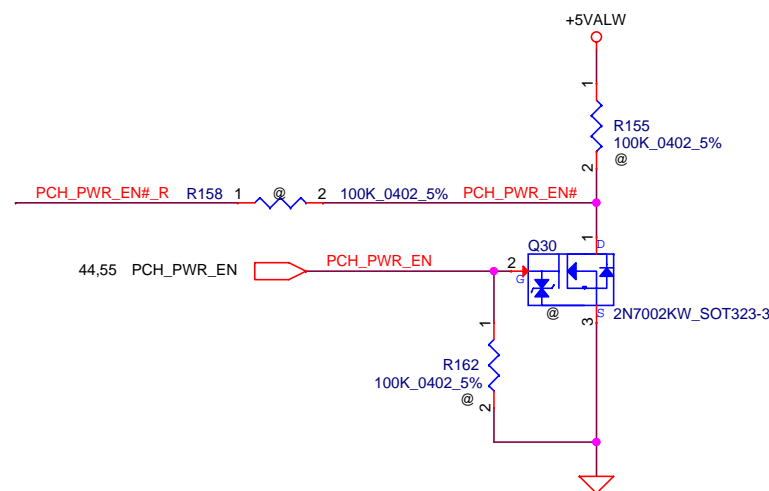
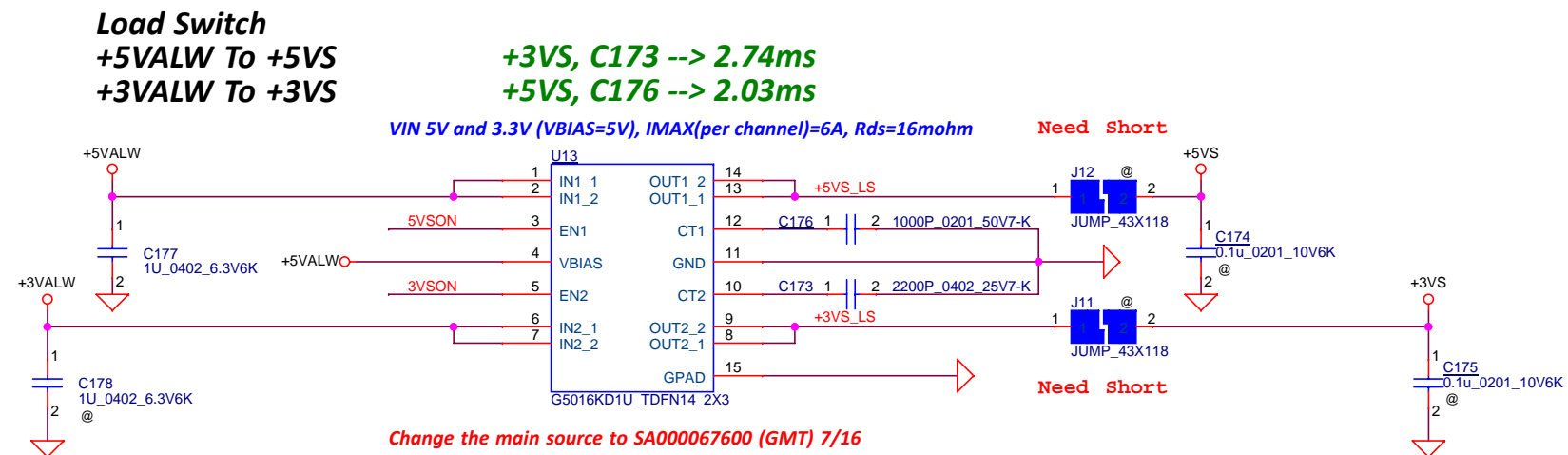
Right Side USB2.0 Port X 2 (USB/B)




TP/B Connector

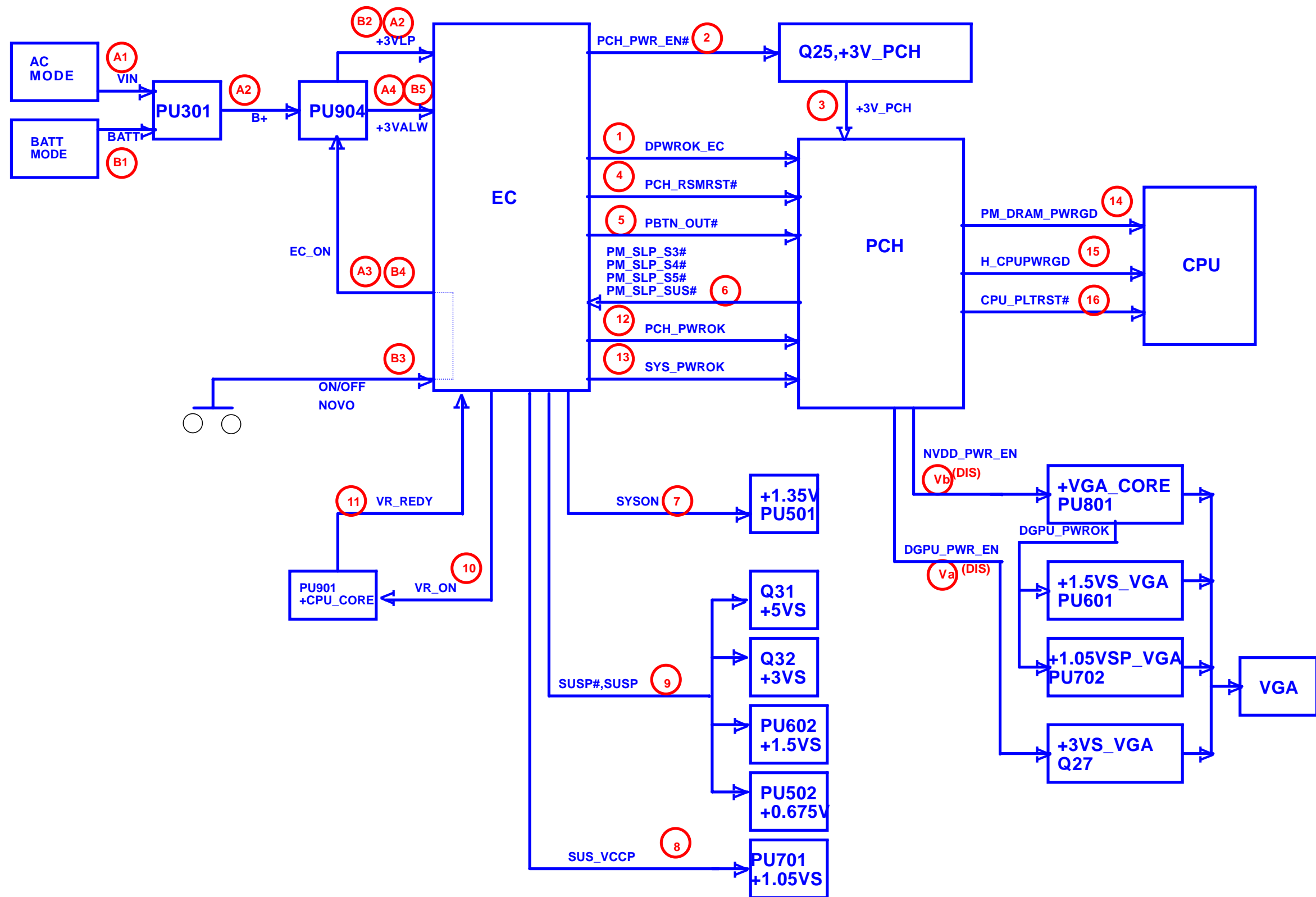


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08/29: Need double check enable signal and the resistance

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WWW AliSaler Com

PCB Fedical Mark PAD

FD1

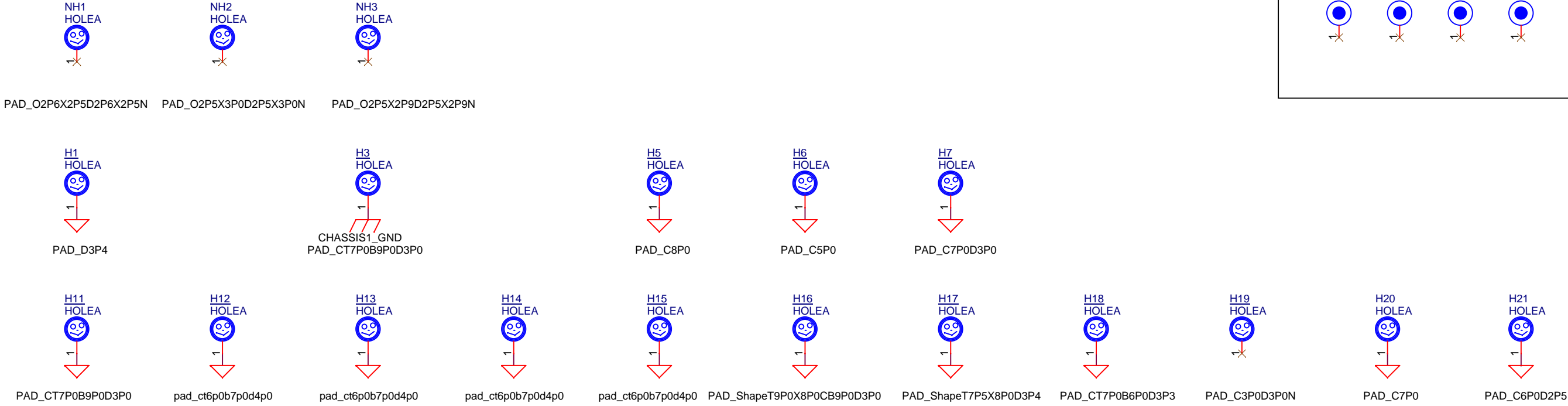
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FD3

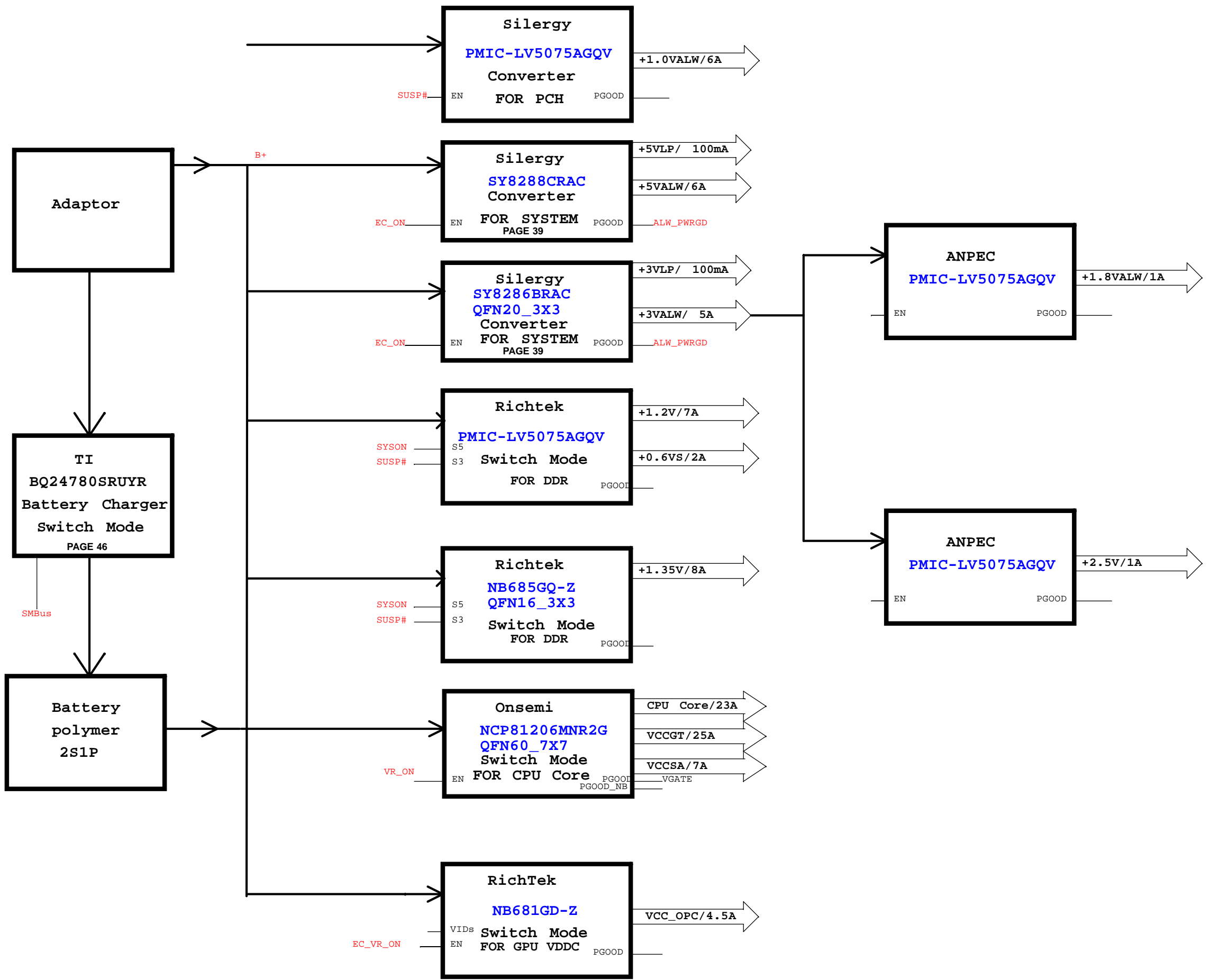
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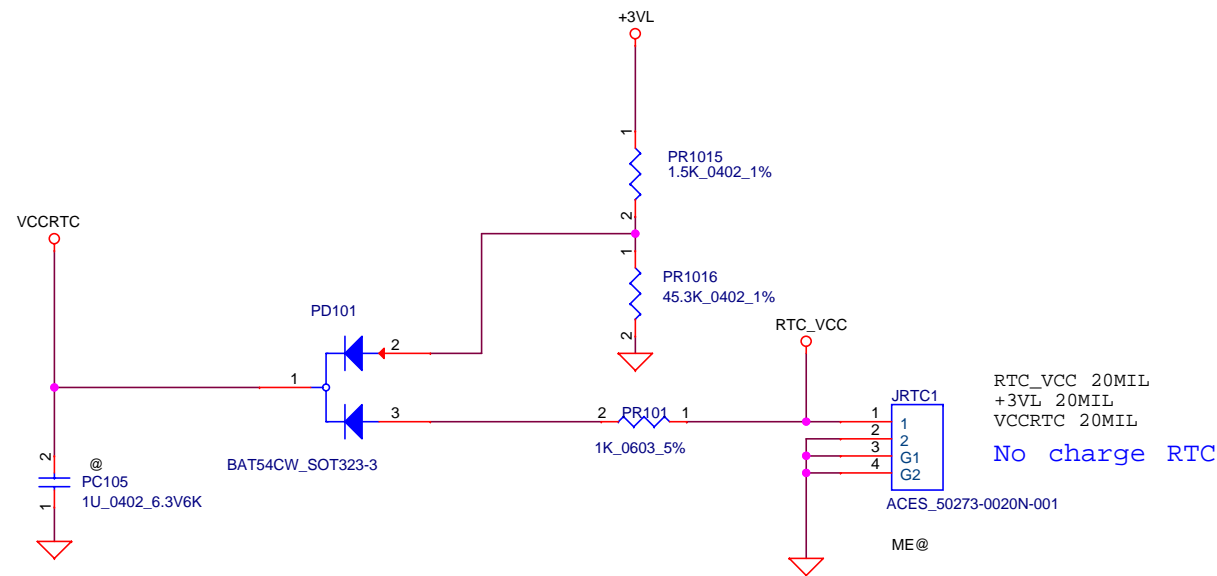
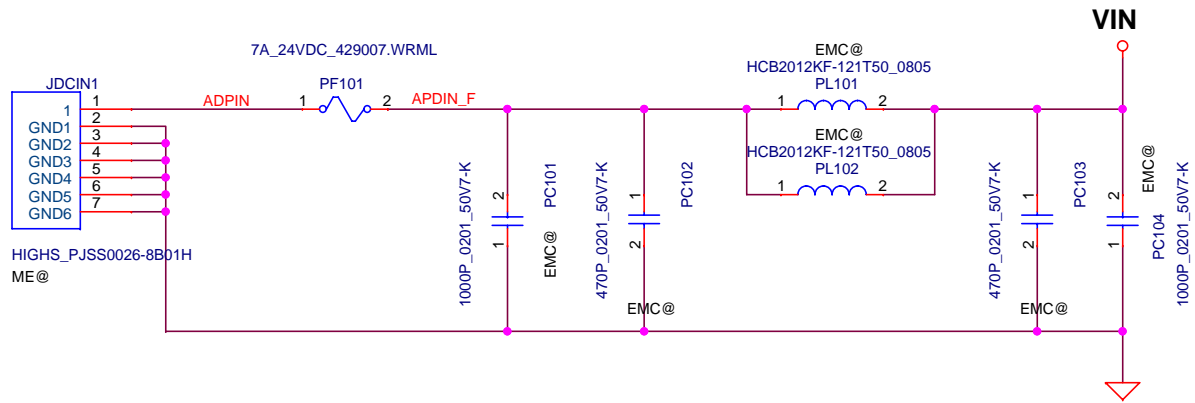
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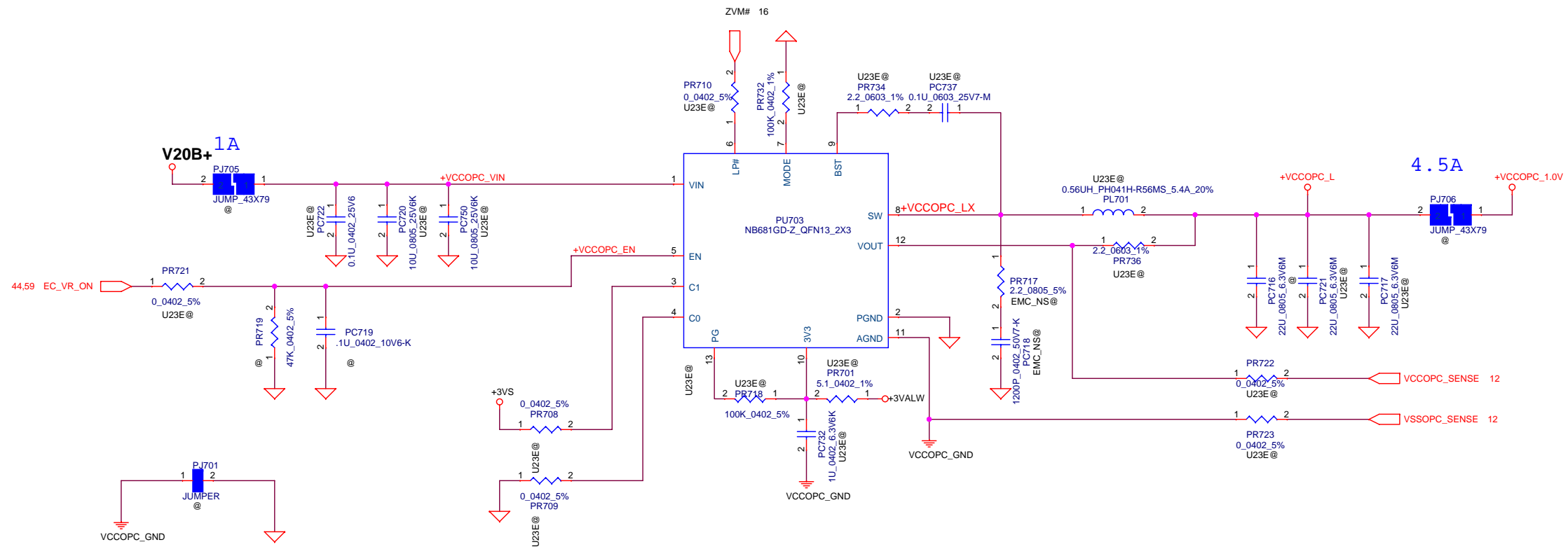
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